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FINAL REPORT

SATELLITE DATA TRANSMISSION (SDT) REQUIREMENT

PREPARED FOR

NASA GODDARD SPACE FLIGHT CENTER
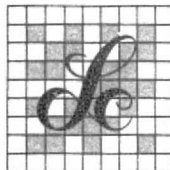GREENBELT, MD 20771

TECHNICAL MONITOR: TOM ROBERTSON

CONTRACT NO. NAS 5-27510

APRIL, 1984

LinCom Corporation

P.O. BOX 15897, LOS ANGELES, CALIFORNIA 90015   TR-0484-8219

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PREPARED BY

C. M. CHIE
M. WHITE
W. C. LINDSEY

LINCOM CORPORATION
P.O. BOX 15897
LOS ANGELES, CA   90015-0897

APRIL, 1984

TR-0484-8219

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EXECUTIVE SUMMARY

Two modulation techniques have been identified for the SDT program. The first technique is proposed by Motorola and is called serial minimum shift keying divide by two (SMSK/2). Figure 1 is the predicted performance of SMSK/2. The region of interest is around a symbol error rate of 10^{-4} which gives a decoded bit error rate of 10^{-7} or smaller. From Figure 1, it can be observed that a 3.7 dB margin is available at the reference system CNR ratio. Also notice that the SMSK/2 is relatively insensitive to carrier phase jitter.

The predicted performance of the second technique, octal phase-shift keying (8PSK), is shown in Figure 2. At an rms carrier phase jitter of 2 degrees, the predicted margin is 2.6 dB. Notice that the 8PSK modem must be equalized and it is rather sensitive to rms phase jitter.

The required symbol error rate of 10^{-4} predicted was based on the use of threshold decodable convolutional codes, our prime coding technique candidate. The other prime coding candidate is the use of multiplexed sequentially decoded convolutional codes which can reduce the required SER to 1.04×10^{-3}, or roughly 2.6 dB additional system CNR margin.

The final selection of the modulation scheme therefore depends on a tradeoff between cost and performance (hardware loss and fading margin to be allocated). Table I is a summary of the SDT modem/codec selections to aid in making this decision.

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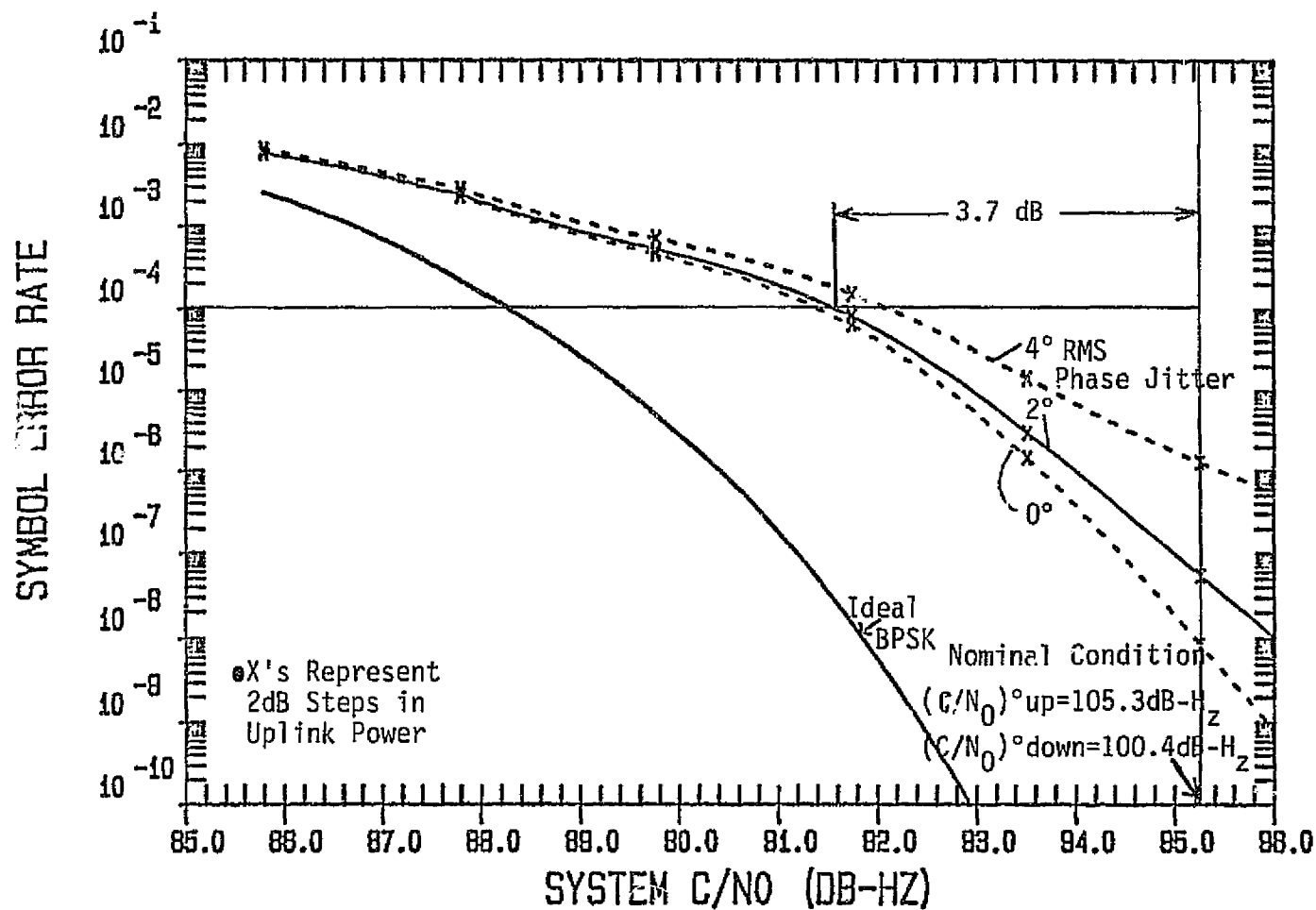
Figure 1. Simulated Performance of SMSK/2 at 97.1 Msps (85 Mbps with rate 7/8 coding)
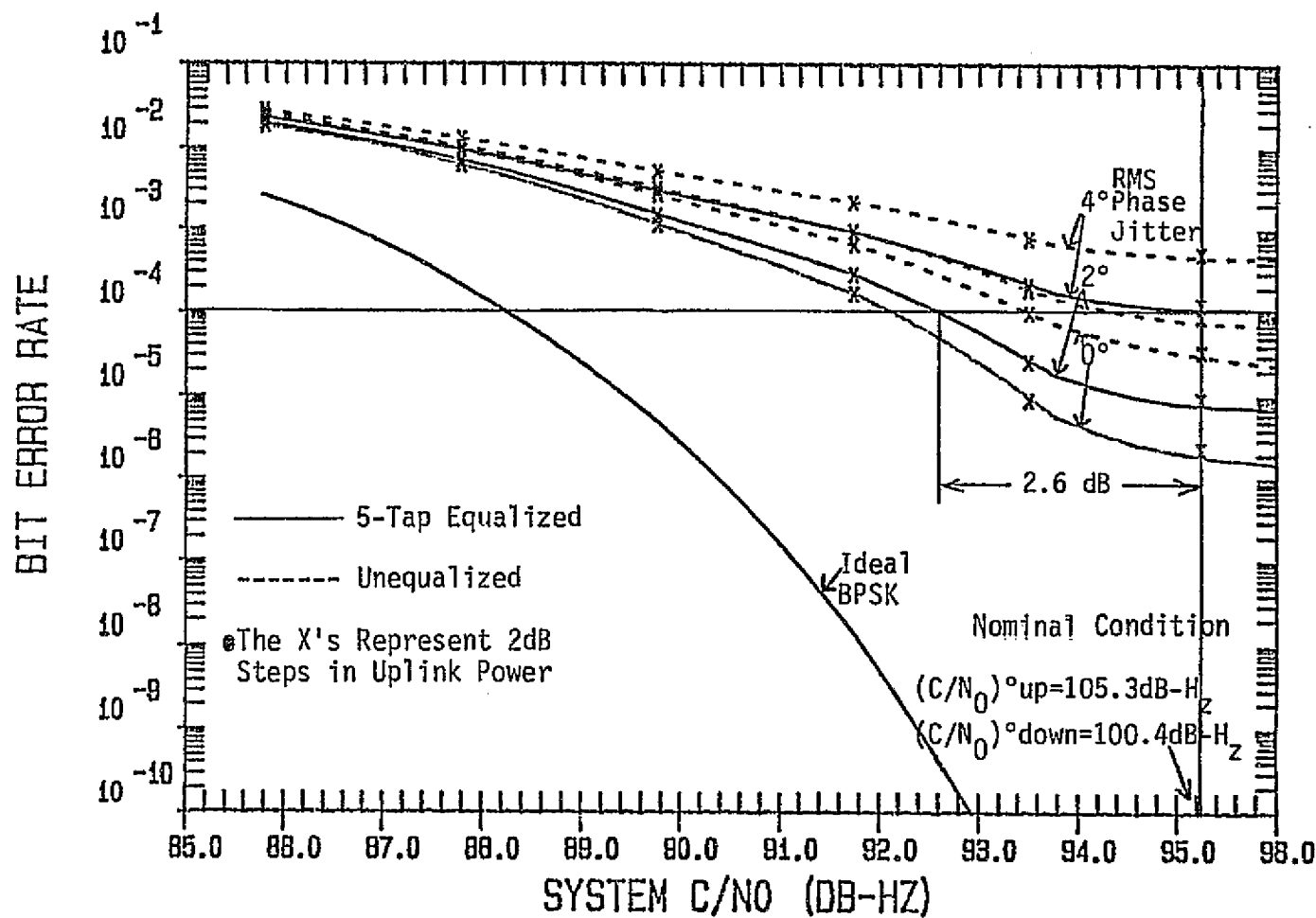
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Figure 2. Simulated Performance of 8PSK at 97.1 Msps (85 Mbps with rate 7/8 Coding)

Table I. Candidate SDT Modem/Codec Selection Summary.

Modem	Motorola SMSK/2	8PSK
Performance (Margin)	3.7 dB	2.6 dB
Hardware Loss	Low	Medium/High
ROM* Cost	2M	0.5-1M
Technology	New	Maturing

*Rough Order of Magnitude (ROM)

Codec	Threshold Decodable Convolutional Codes	Viterbi/Sequentially Decoded Convolutional Codes
Performance (AWGN Codng Gain)	3 dB	4.9 dB
Hardware Loss	Negligible	Negligible
ROM Cost	200 - 300 K	300 - 500 K
Technology	Matured	Maturing

1.0 Introduction

The objective of this study effort is to develop the requirements for an 85 Mb/s modem/codec to operate in a 34 MHz C-Band domestic satellite transponder at a system carrier-to-noise power ratio of 19.5 dB. Figure 1-1 shows the intended application of the modem/codec. Since the available channel bandwidth and downlink power are fixed, this represents a loss of 2.3 dB in E_b/N_0 and a simultaneous reduction of 41% in the channel BT product, with respect to an existing 50 Mbps link operation. The major technical challenge in the SDT program is therefore to select the combination of modulation and coding techniques that can meet this more stringent performance requirement. The technical approach for modulation/coding tradeoffs selected by LinCom/Motorola in the SDT study is based on simulating the SDT link with all the pertinent modem and channel parameters. The results from the simulation form the basis for selecting the optimal modem/codec implementation technique.

This report is organized as follows. The rest of Section 1 is devoted to a discussion of the characteristics of a satellite channel and the approach adopted by LinCom for the SDT modem/codec selection. Section 2 addresses the SDT path simulation model. A comparison of the measured data and simulation results of the existing 50 Mbps link is used to verify the simulation technique. Section 3 discusses the various modulation schemes that have been screened for the SDT. The simulated performance of the two prime candidates, 8PSK and Motorola SMSK/2, are also given. Section 4 documents the selection process that leads to the candidate codec techniques. The technology assessment of the modem/codec candidates is given in Section 5. Finally, Section 6

Figure 1-1.   SDT OVERVIEW
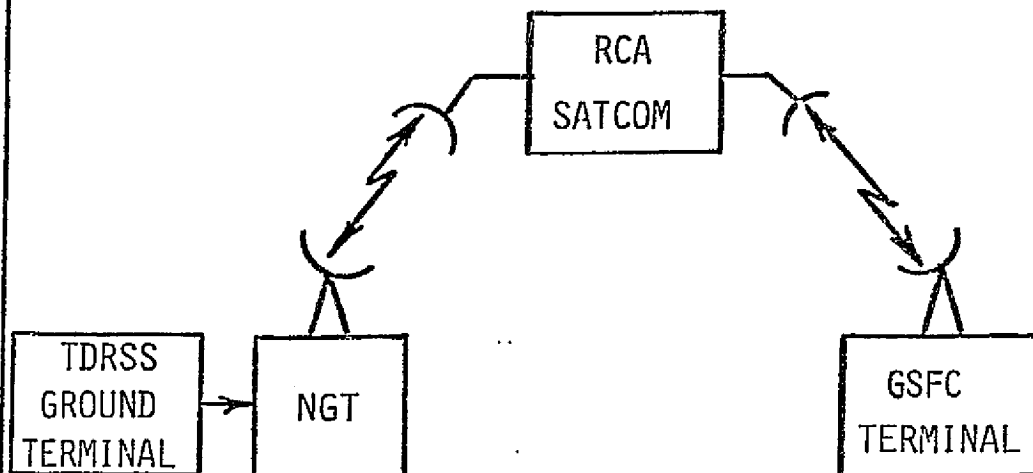
- PURPOSE IS TO PROVIDE HIGH RATE DIGITAL DATA
  TRANSMISSION CAPABILITY FOR TDRSS USER DATA
  FROM NASA GROUND TERMINAL (NGT)
  TO GSFC VIA AN RCA AMERICOM DOMESTIC SATELLITE
  TRANSPONDER (C-BAND)

- CURRENT CAPABILITY IS 50 Mbps

- OBJECTIVE FOR SDT STUDY IS TO UPGRADE DATA
  RATE TO 85 Mbps

gives a cost estimate of the modems and codecs.

1.1 Satellite Data Transmission (SDT) Channel Model

A simplified functional diagram of the SDT system, including the transmit and receive Earth stations, is illustrated in Figure 1-2. Illustrated in this diagram are the key contributors which affect system performance. These include:

- o   Choice of Coding

- o   Choice of Modulation

- o   Transmit Modem Filter

- o   Transmit Filter Chain

- o   Earth Station High Power Amplifier (HPA) Nonlinearity

- o   HPA Output Bandpass Filter

- o   Adjacent Channel Interference (ACI)

- o   Adjacent Channel Multipath

- o   Satellite Input Channel Filter

- o   Satellite TWT Nonlinearity

- o   Satellite TWT Output Filter

- o   Receiver Filter Chain

- o   Receiver Modem Filter

- o   Receiver Carrier Recovery

- o   Receiver Clock Recovery

- o   Receiver Decoder

The user data are suitably encoded and fed into the modulator. The modulated carrier is passed through the modem filter in order to shape the transmitted pulses so as to minimize the effects of adjacent channel interference. This pulse shaping creates intersymbol interference (ISI). This filtered signal is upconverted to the uplink frequency and

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SATELLITE

PREAMP

BANDPASS FILTER

LOCAL OSCILLATOR

DOWN CONVERTER

BANDPASS FILTER

LOCAL OSCILLATOR

UPCONVERTER

BANDPASS FILTER

TWTA

ADJACENT CHANNELS

DIPLEXER

RECEIVE BANDPASS FILTER

COMMON JUNCTION

TRANSMIT BANDPASS FILTER

EARTH STATION

EARTH STATION

EARTH STATION

EARTH STATION

MODEM

ENCODER

MODULATOR

MODEM FILTER

LOCAL OSCILLATOR

UPCONVERTER

BANDPASS FILTER

FREQUENCY SOURCE

BANDPASS FILTER

HPA

TRANSMIT EARTH STATION

RECEIVE EARTH STATION

PREAMP

DOWN-CONVERTER

BANDPASS FILTER

MODEM FILTER

EQUALIZER

LOCAL OSCILLATOR

MODEM

CLOCK RECOVERY

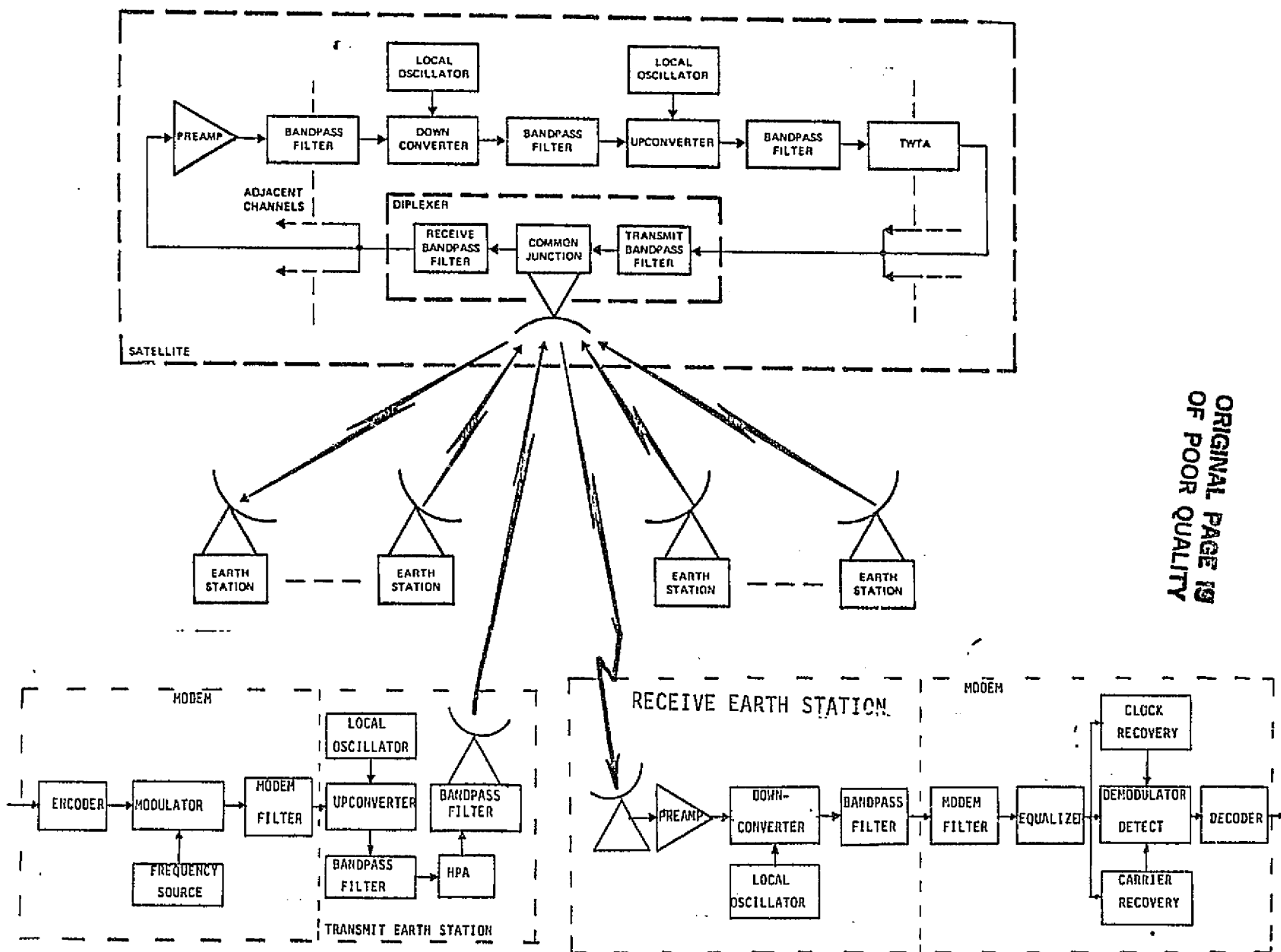DEMODULATOR DETECT

CARRIER RECOVERY

DECODER

Figure 1-2.   SDT System Functional Block Diagram.

filtered to reduce spurious products. The uplink signal is then power amplified by the earth station HPA and, in general, will be passed through the HPA output filter to minimize adjacent channel interference. However, for constant envelope signals this filter is not necessary and its absence will result in hardware and EIRP savings. This filter, along with the modem filter, establishes uplink bandwidth and, in conjunction with the bit duration (T) establishes the channel BT product.

As a result of the transmit modem filtering, linear distortion on the signal is created; i.e., the signal contains amplitude modulation (AM). Due to the AM-PM characteristics of the HPA, phase noise will be generated on the output signal. In addition, AM to AM conversion takes place in the HPA due to the AM to AM characteristic. These nonlinear distortions are of great concern as far as system performance is concerned. They affect the information content of the signal within its assigned channel bandwidth. In addition, since the HPA broadens the signal spectrum which spills over to the neighboring frequencies, adjacent channels are also affected. It is important to assess the degradations on system performance and minimize their effects.

The uplink signal (and adjacent channel signals) are received by the satellite antenna and processed by the satellite input filters as indicated in Figure 1-2. A separate filter is used for each of the N users. As illustrated, the signal is downconverted to an IF frequency. After further filtering and amplification the IF signal is upconverted and passed through a wideband filter to reduce spurious products. The signal is then amplified by the satellite TWT transmitter and passed through the satellite output filter. Since the uplink signal

contains AM (due to uplink noise, adjacent channels, and uplink filters) phase modulation is generated by the AM to PM transfer characteristic of the saturated satellite TWT. In addition, AM to AM distortion takes place due to the TWT amplitude transfer characteristic. Thus, these linear and nonlinear signal distortions further impair system performance. Equalization of the channel group delay characteristic is of concern in the modem design.

The downlink signal is received by the earth station receiver and demodulated as indicated in Figure 1-2. The receiver modem filter is selected so as to reduce the intersymbol interference created by bandlimiting the signal in the transmit modem filter. Selection of these two filters must not be carrier out independently since the linear and nonlinear distortions just discussed must be optimally corrected to achieve near optimum end-to-end system performance. In view of the high signal-to-noise ratio operation and the absence of dynamics, carrier and clock recovery do not appear to be of great concern here. However, one must be careful to accommodate the effects of pattern noise arising from the small BT constraint in their designs. Finally, the demodulated symbols must be decoded to recover the transmitted data.

1.2 Technical Approach

Figure 1-3 shows LinCom's recursive approach for accomplishing the definition of advanced signal processing and coding techniques required for the modem/codec. Based on LinCom's modulation/coding tradeoff experience and Motorola's advanced modem implementation experience, candidate modulation/coding techniques are first identified. The modulation/coding technique is then evaluated using LinCsim (LinCom's SDT simulation) based on a simplified link scenario with:
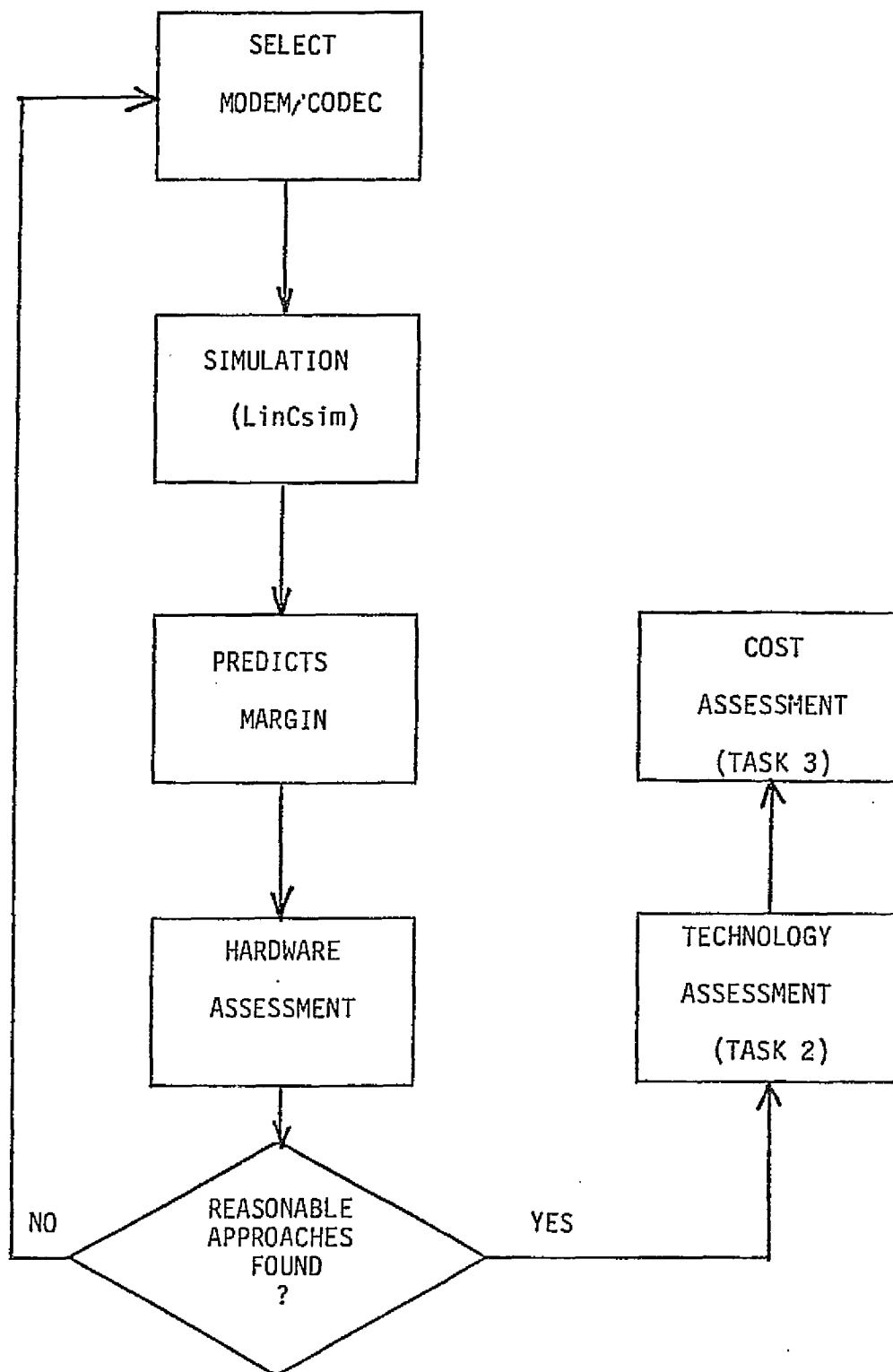
Figure 1-3. Technical Approach

o   Earth station RF specifications (HPA, channel filter mask)

o   Transponder specifications (TWT, transponder filter mask)

o   Idealized, equalized modem filters

o   No signal distortions (gain imbalance, phase imbalance, etc.

o   Equivalent thermal noise for ACI

Based on the simulated margin, promising candidates are then evaluated for hardware complexity. If the technique still appears to be practical at this point the simulation is modified to include more refined models including adaptive equalization and carrier recovery. Using the refined simulation model, the simulated performance of the candidate modem should track the hardware implementation to within 1-2 dB.

This process continues until one or more candidate schemes are found to be meeting the SDT requirement with a reasonable margin. At this point, the hardware complexity of the modem/codec candidates(s) are examined. If the hardware requirements are not excessive, the design(s) are then assessed in terms of technology and cost.

2.0 SDT Transmission Path Simulation Model

Since the coding and modulation tradeoffs for the SDT are based upon the results of computer simulation, the transmission path must be carefully modeled in the software. A rather general model typical of C-band satellite transmission was used in the early stages of this work. The parameter selections are based on a worst-case interpretation of the RCA satellites F1 & F2 specification associated with the earlier 50 Mbps modem development. As this work progressed, the transmission path model was further refined as more information on the satellite link characteristics were provided by RCA.

The preliminary simulation model for the SDT transmission path is

shown in Figure 2-1. The effects of the uplink noise and interference are modeled by an equivalent composite downlink noise determined by the system carrier-to-noise power ratio of 19.5 dB specified in the RFP. (A noise bandwidth of 33.5238 MHz is assumed.) The effects of power backoff of the nonlinear amplifiers (HPA and TWT) will be reflected by adjusting this system CNR accordingly.

The HPA and TWTA are modeled by the AM/AM and AM/PM characteristics shown in Figure 2-2. The characteristics shown are based on curve-fitting to data measured on a typical C-Band TWT amplifier. The AM/PM conversion is about 4°/dB as specified by RCA.

For the purpose of the preliminary investigation of waveform candidates, the filters in Figure 2-1 are modeled as perfectly equalized Chebyshev filters with 1 dB ripple. The parameters used in the simulation are summarized in Table 2.1.

Based on the new amplitude response and group delay characteristics for the RCA satellite F1R supplied in June, 1983, by Rick Langhans of RCA, the filter models are modified for the LinCom simulation. The old and new filter parameters are compared in Table 2.2. The satellite input channel filter is modeled to resemble the RCA measurement which represents the overall link performance (including the earth terminal filters). Bandwidths and pole-orders of the rest of the filters in the link model are adjusted accordingly.

Measured amplitude response and group delay characteristics are compared with the simulation models in Figures 2-3 and 2-4. The satellite input channel filter is modeled as a 3-pole Chebyshev filter with 0.2 dB ripple. The group delay is approximated by a parabolic group delay over the center 28 MHz band. Based on inputs from Jim
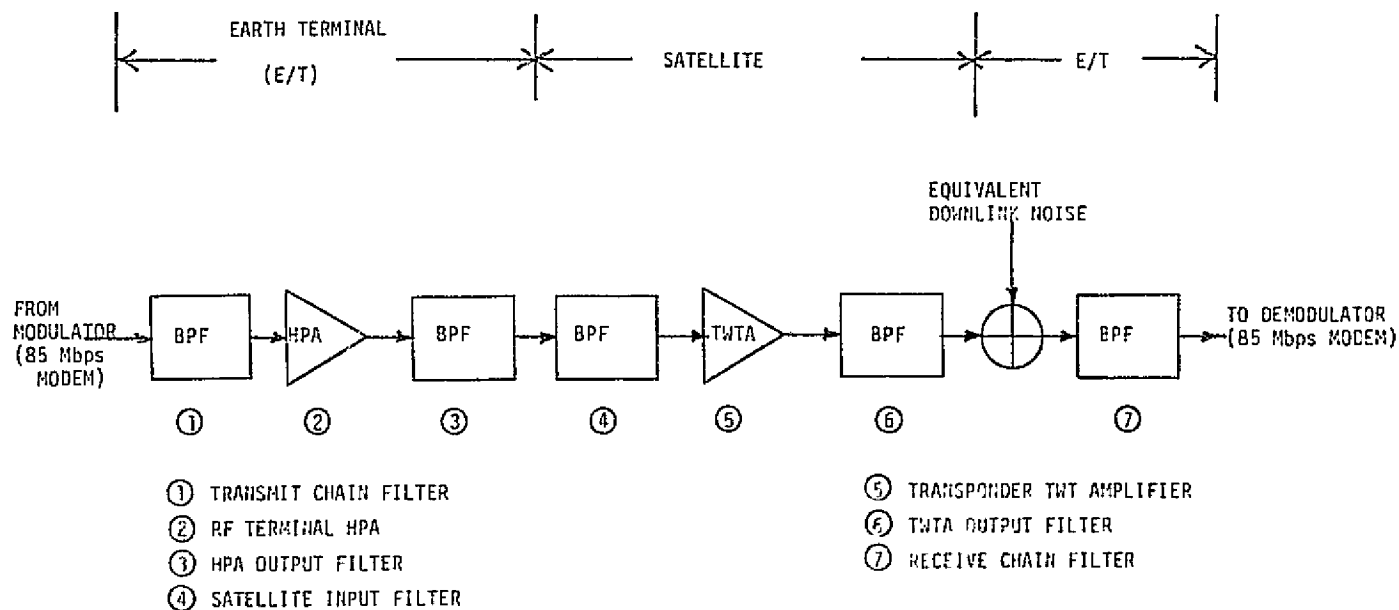
LinCom

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Figure 2-1.   SDT Transmission Path Model.
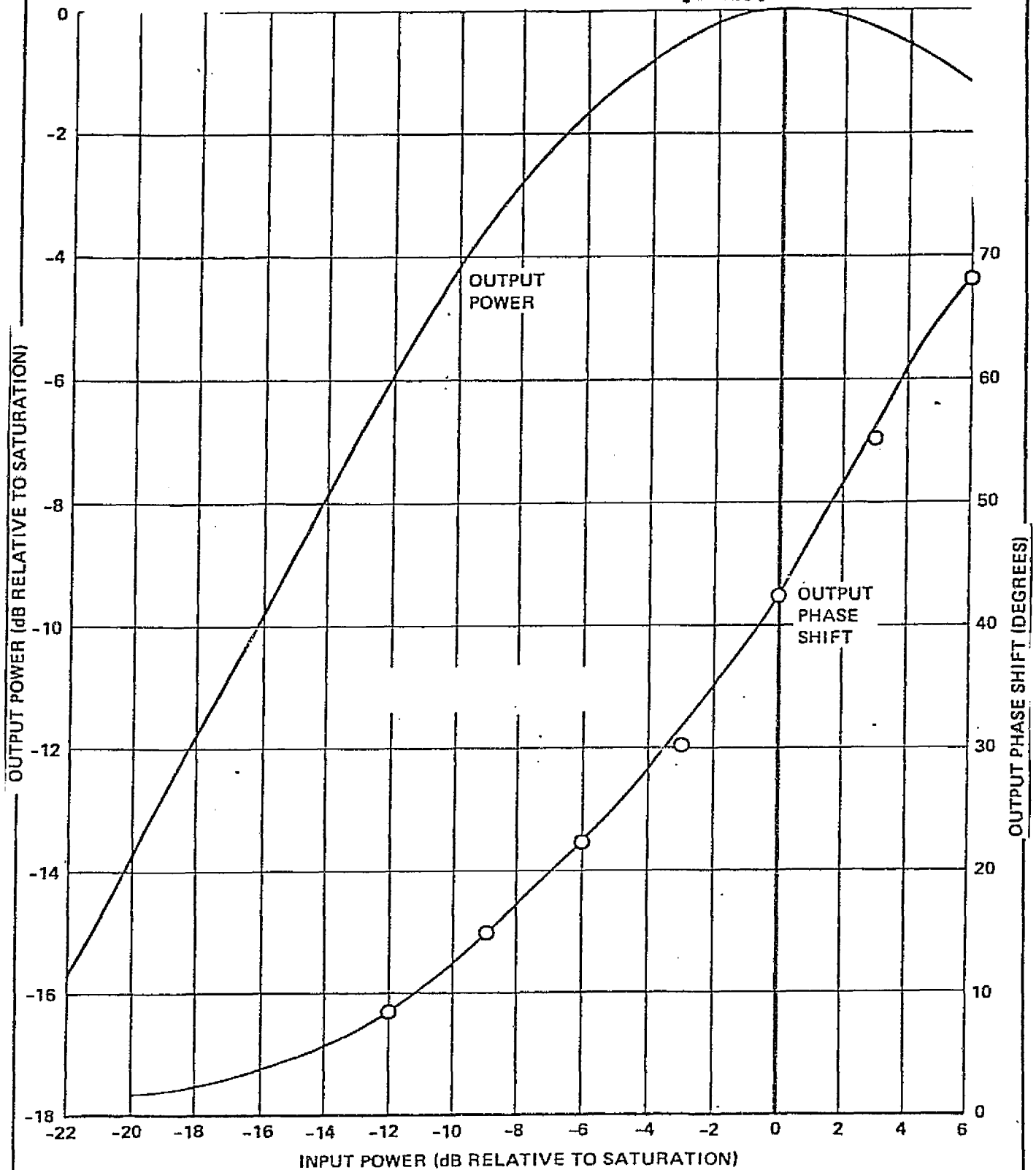
LinCom

Figure 2-2.   Model Nonlinear Amplifier Input-Output Characteristics.

Table 2.1. Simplified Simulation Model for Satellite Transmission
            Path.

ITEM	MODEL
TRANSMIT CHANNEL FILTER ①	W = 38 MHz, 4-POLE*
HPA ②	INPUT BACKOFF 6-12 dB**
HPA OUTPUT FILTER ③	W = 38 MHz, 4-POLE*
SATELLITE CHANNEL FILTER ④	W = 34 MHz, 6-POLE*
TRANSPONDER TWTA ⑤	INPUT BACKOFF (AROUND 3 dB) TO BE OPTIMIZED**
TWTA OUTPUT FILTER ⑥	W = 34 MHz, 3-POLE*
RECEIVE CHAIN FILTER ⑦	W = 38 MHz, 4-POLE*

NOTES: * Chebyshev Filter, ideally equalized with 1 dB
           ripple and 3 dB RF bandwidth W.

         **See Figure 2-2 for AM/AM and AM/PM characteristics
           model.

Table 2.2. Comparison of New Filter Models Based on FIR Data
Supplied by RCA on June 6, 1983 with Old Filter Models

	Old Model[1]	New Model[2]
Transmit Channel Filter	W=38 MHz 4-pole	W=42 MHz 4-pole
HPA Output Filter	W=38 MHz 4-pole	W=42 MHz 4-pole
Satellite Input Channel Filter	W=34 MHz 6-pole	W=39 MHz 3-pole
TWT Output Filter	W=34 MHz 3-pole	None
Receive Chain Filter	W=38 MHz 4-pole	W=42 MHz 4-pole

[1] Chebyshev with 1 dB peak-to-peak ripple ,   3 dB Bandwidth W

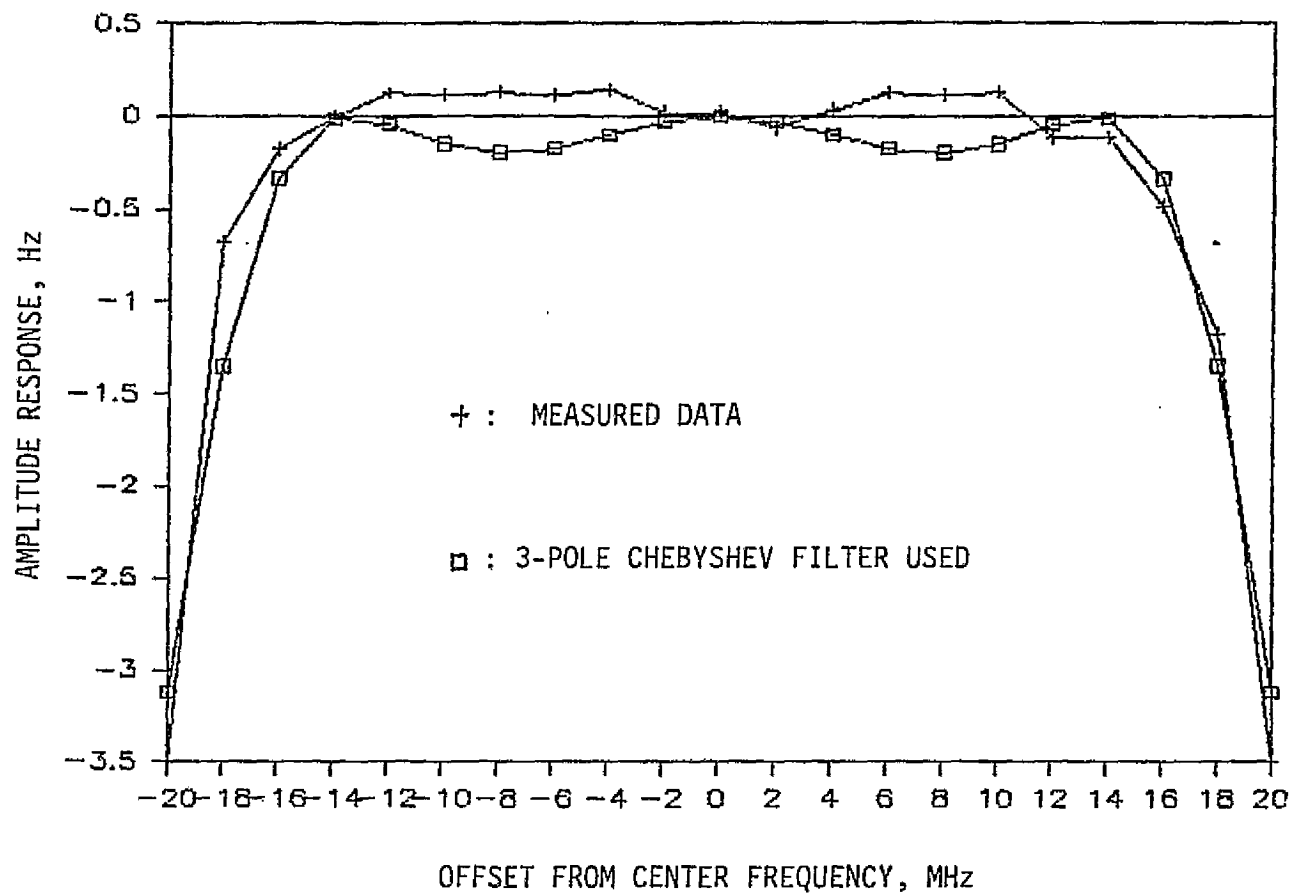[2] Chebyshev with 0.2 dB peak-to-peak ripple ,   3 dB Bandwidth W
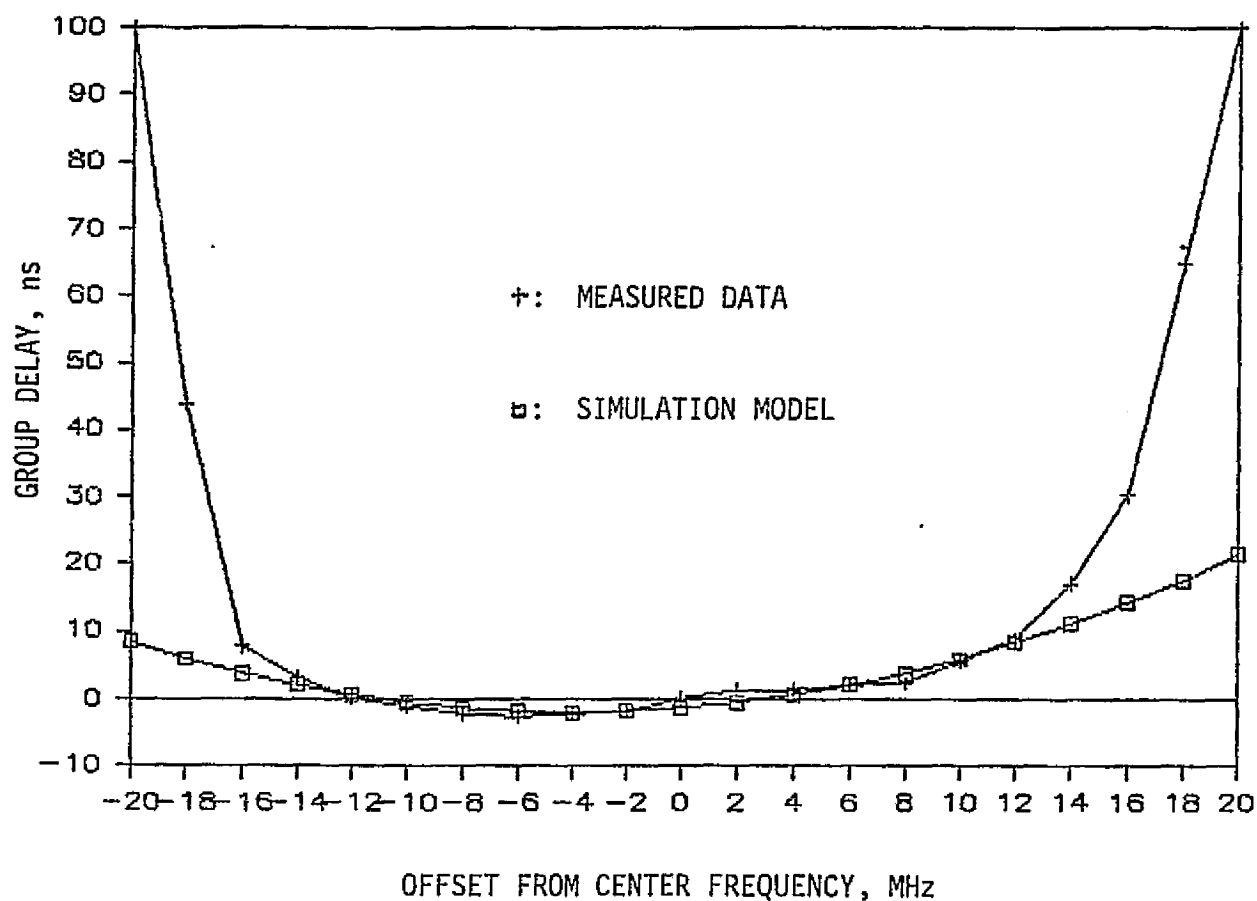
Figure 2-3. Amplitude response

Figure 2-4. Group Delay Response

O'Donnell of RCA, an additional sinusoidal group delay component (period = 14MHz, peak value = 3.5 ns) was incorporated in February 1984.

The last major refinement of the transmission model was based on RCA inputs on Dec. 1983. The changes were on the modeling of the earth terminal high power amplifier (HPA), the replacement of the satellite TWT amplifier (TWTA) by a solid state power amplifier (SSPA), and the uplink, downlink and system carrier-to-noise power ratios.

Figure 2-5 shows the new SSPA amplifier AM/AM and AM/PM characteristics provided by RCA as compared to the old TWTA characteristics. The 0 dB reference point on the attached SSPA characteristics corresponds to a worst case 37 dBW Satellite EIRP over Goddard. The earth station G/T at Goddard is 31.5 dB/°K. Assuming a free space loss of 196.7 dB, the downlink C/N_0 is 100.4 dB-Hz at that reference point. This is computed by

C/N_0 = EIRP (37) - Free Space Loss (196.7)

   + G/T (31.5) - Boltzman's Constant (-228.6).

At the 0 dB reference point for the SSPA, the uplink earth station klystron operates at a sufficient backoff (8-10 dB output backoff) and can be assumed to be linear so that the AM/AM and AM/PM characteristics of the klystron can be ignored. The drive level of the klystron only affects the power backoff of the SSPA. Assuming an uplink transmit EIRP of 80.7 dBW, a free space loss of 200 dB, and a satellite G/T of -2.0 dB/°K, the uplink C/N_0 is 105.3 dB-Hz defined at the 0 dB reference point. Table 2.3 summarizes the satellite link budget with the new SSPA.

2.1 Verification of the Simulation Technique

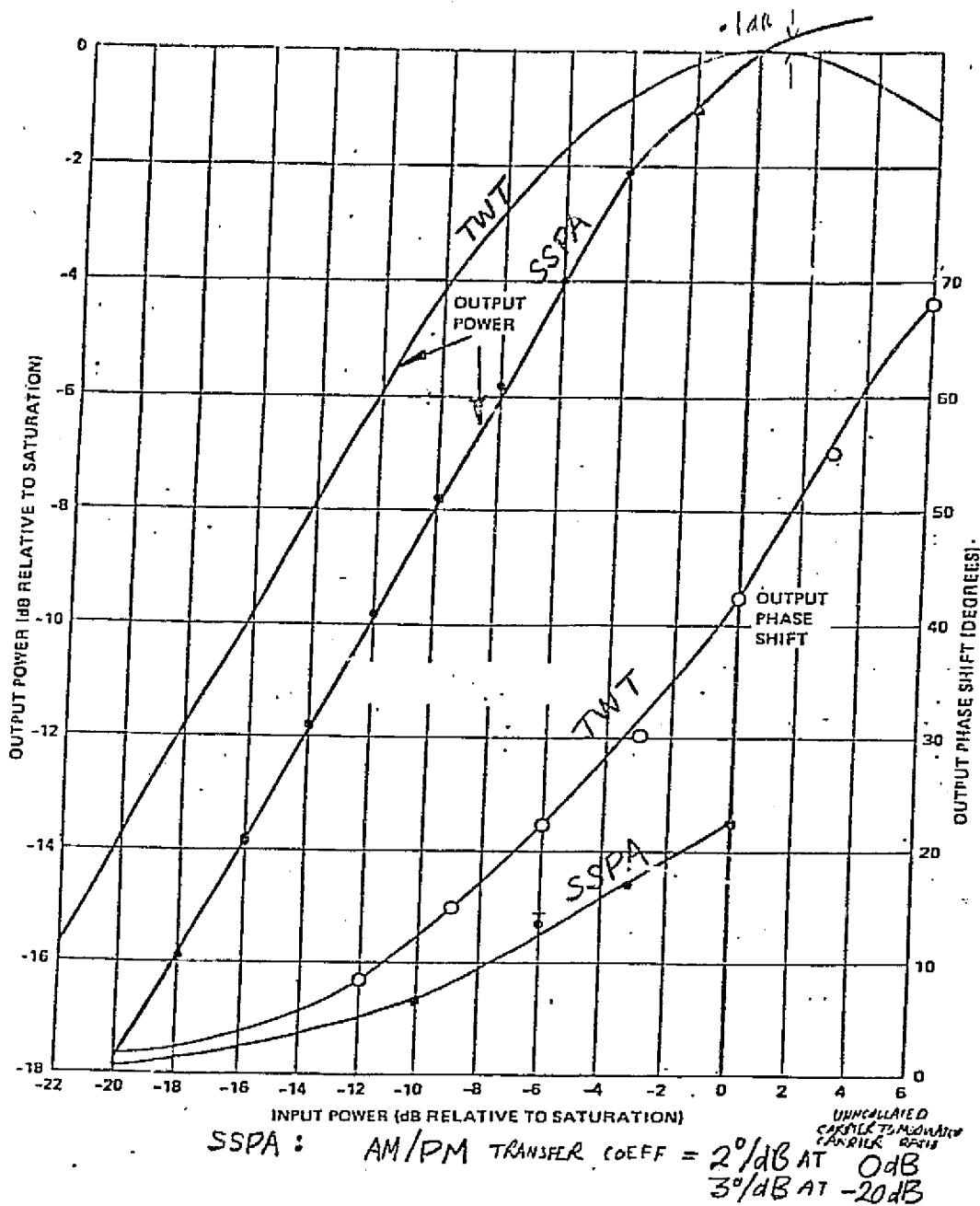As a means of providing further verification of the LinCsim model,

Figure 2-5. Comparison of TWT and SSPA

TABLE 2.3. <u>COMPARISON OF NEW AND OLD STATELLITE LINK BUDGETS</u>

PARAMETERS	OLD	NEW
UPLINK C/N_0 (dB-Hz)	105.3	105.3
DOWNLINK C/N_0 (dB-Hz)	98.8	100.4
INTERFERENCE C/N_0 (dB-Hz)	97.5	97.5
SYSTEM C/N_0 (dB-Hz)	94.7	95.2
SYSTEM E_b/N_0 (dB)	15.4	15.9

<u>Note</u>: C/N_0 is based on saturated TWT (old) or SSPA at reference
operating point (new). Required E_b/N_0 at 10^{-7} is 11.3 dB
for ideal BPSK.

it is of interest to compare the LinCsim results with the existing 50 Mbps modem measured data. The following is a list of the salient features of the current system:

Modem   Aydin Model 2708M,D

Modulation   QPSK

Transmit/Receive Pulse   Square Root of Nyquist
Shaping Filter

Baud Rate (Coded)   28.571429M baud
                     (1 baud = 1 QPSK symbol/sec)

Coding Employed   Convolutional Encoding
                     with threshold decoding,
                     hard quantized

Coding Rate   7/8

Figure 2-6 shows the measured data and the accompanying simulation results for the coded symbols. A linear HPA was used for the earth terminal and a TWTA model was used for the satellite transponder. At the coded symbol error rate of interest (between 10^{-3} and 10^{-4} which yields a decoded BER of 10^{-7}), the difference between the simulation and measurement is about 3.1 dB. According to Jim O'Donnell of RCA, the back-to-back modem performance is approximately 1-2 dB away from theoretical (which can be improved if required). Additionally, there was no attempt to equalize the satellite channel while the measurement data was taken. This can make a difference of a couple dBs. The RCA practice is understandable since the existing link margin is more than sufficient to meet the link performance requirement. With these facts in mind, it is estimated that the LinCsim results should be able to track to within 1-2 db of the hardware performance.

3.0 Modulation Selection

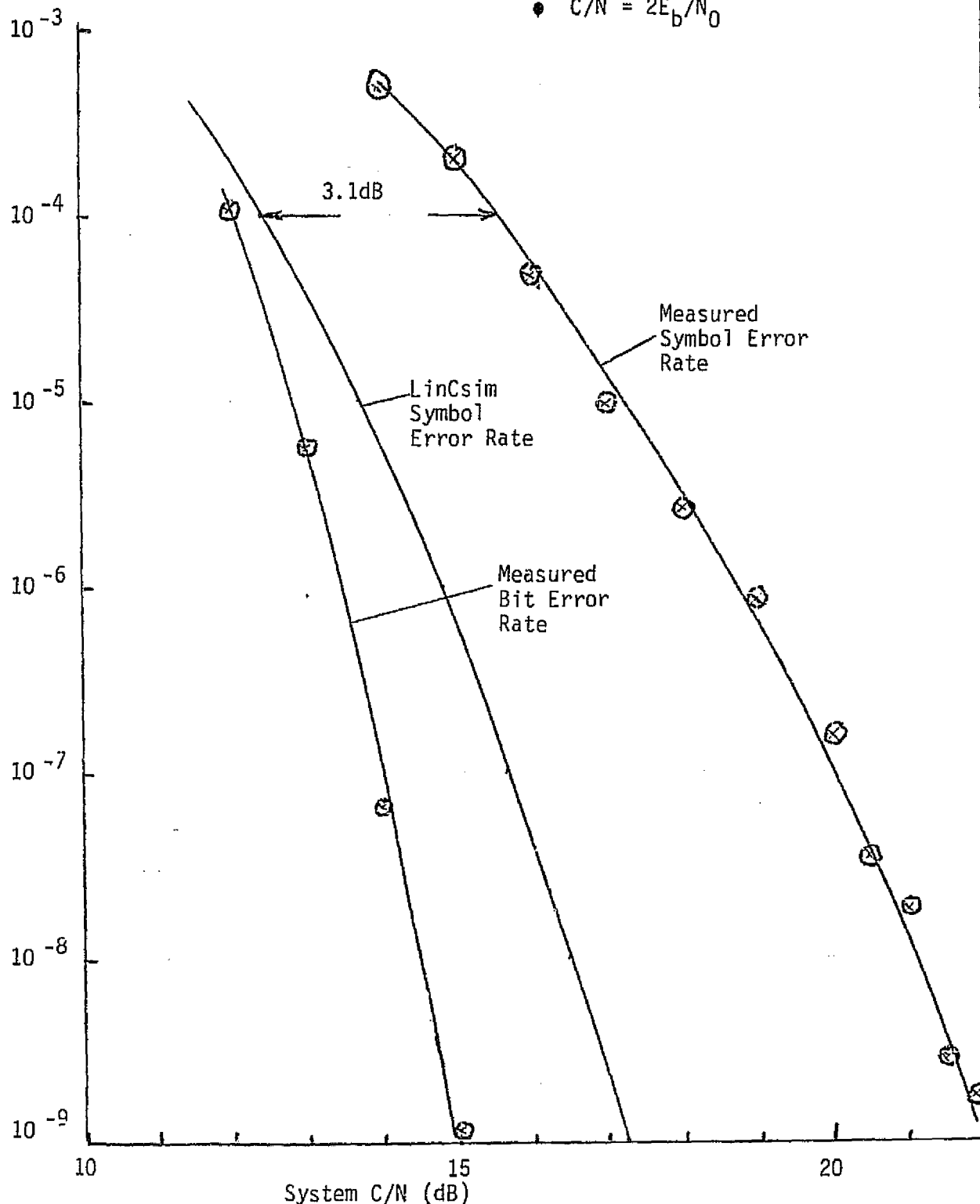The transmission channel for SDT consists of a severely bandlimited

Figure 2-6. Comparison Between Simulation and RCA Measurement Data for 50 Mbps Modem.

nonlinear channel (HPA and satellite nonlinearity) with additive
Gaussian noise and adjacent channel interference on both the uplink and
the downlink. The required data rate of 85 Mbps through a 34 MHz
channel results in a BT product of 0.4. This is significantly less than
BT ≈ 1 for a typical satellite transmission system. The total system
C/N of 19.5 dB yields a E_b/N_0 of 15.5 dB, which represents a mere 4.2 dB
margin from ideal antipodal (BPSK) transmission for the specified bit
error rate of 10^{-7}. Under the severe bandlimiting condition and tight
E_b/N_0 budget, the choice of the modulation/coding technique must be
carefully evaluated to ensure that the SDT modem/codec can meet the
required performance.

Since the satellite transponder must operate near saturation to
yield the maximum power output, the modulation schemes to be considered
are limited to the class of constant envelope modulation schemes. This
precludes, for example, the highly efficient 16 QAM signaling format
used for digital microwave radio. Within the class of constant envelope
modulation schemes, the M-ary PSK and continuous phase modulation (CPM)
appear to be the most likely candidates for the SDT requirements. It is
impossible to evaluate each candidate scheme in detail, therefore, we
first seek to weed out the weak candidates by comparing their simulated
performances under an otherwise idealized bandwidth limited channel.
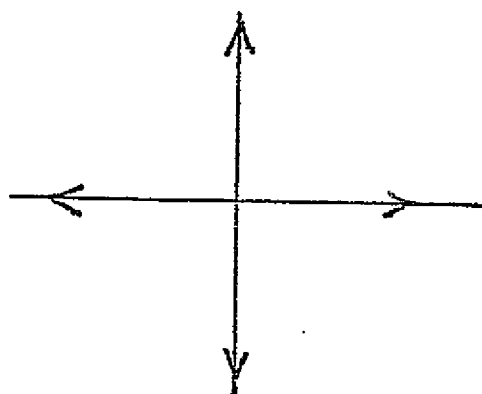
3.1 Modulation Formats Under Consideration

3.1.1 MPSK

The conventional MPSK Modulation signal constellations are shown in
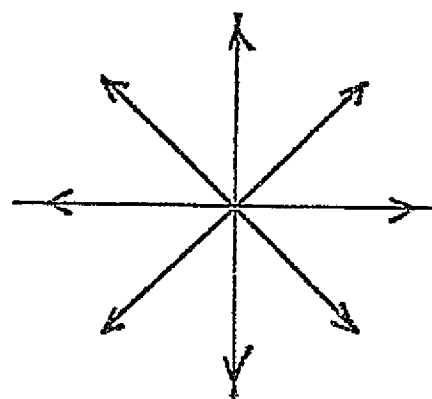Figure 3-1. The tip of each arrow depicts each possible signal vector.

3.1.2 KQPSK

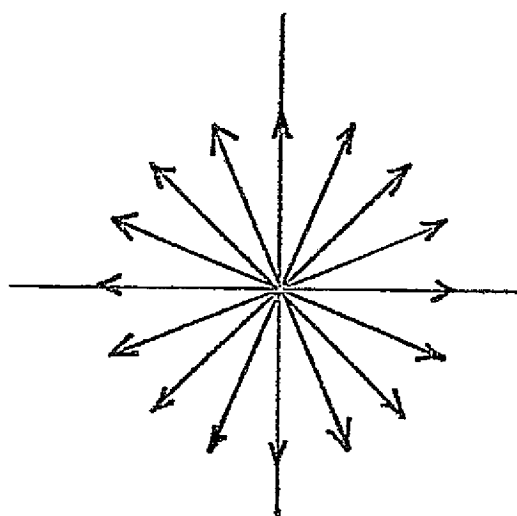The constrained QPSK (KQPSK) is a form of QPSK and is shown in

(a) QPSK

(b) 8PSK

(c) 16PSK

Figure 3-1. Signal Space Representation of MPSK Signals.

Figure 3-2. During data transitions, the signal vector can either stay put or jump to its closest clockwise neighbor. Therefore, only 1 information bit is transmitted per symbol. This modulation waveform is adapted from the Motorola proprietary MSK/2 modem concept.

3.1.3 Motorola MSK/2 (Old Version)

The phase trellis for the MSK/2 is shown in Figure 3-3. The phase of the transmitted signal either increases or decreases linearly by $\pi/4$ over one bit period. (In the standard MSK, the phase of the transmitted signal either increases or decreases linearly by $\pi/2$ over one bit period. Since the MSK/2 scheme modulates the carrier at one half of the frequency of MSK, i.e., $\pi/4T$ vs. $\pi/2T$, MSK/2 has a narrower spectrum). In order to optimize the performance, the demodulator examines 2 consecutive bits to make a one bit decision, which is very close to maximum likelihood detection performance.

3.1.4 GMSK

Gaussian MSK (GMSK) is a form of minimum shift keying (MSK). Its implementation is shown in Figure 3-4. The performance of the modem is determined by the bandwidths of the pre-modulation and the receiver Gaussian filters.

3.2 Spectral Characteristics

The power spectra for the modulation formats considered are compared in Figure 3-6. The normalized horizontal axis is the equivalent one-sided baseband BT product. For 85 Mbps and a 34 MHz bandwidth, this corresponds to 0.2. Since coding involves bandwidth expansion, the channel "bit" rate will be increased by a factor between roughly 8/7 to 4/3 (assuming rate 3/4 and 7/8 codes). The BT product will be between 0.175 to 0.15. The out-of-band power of the modulation
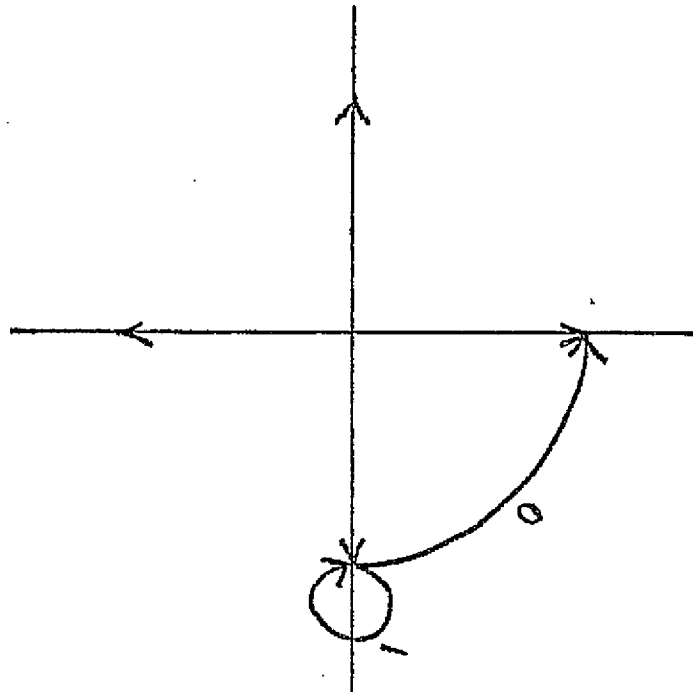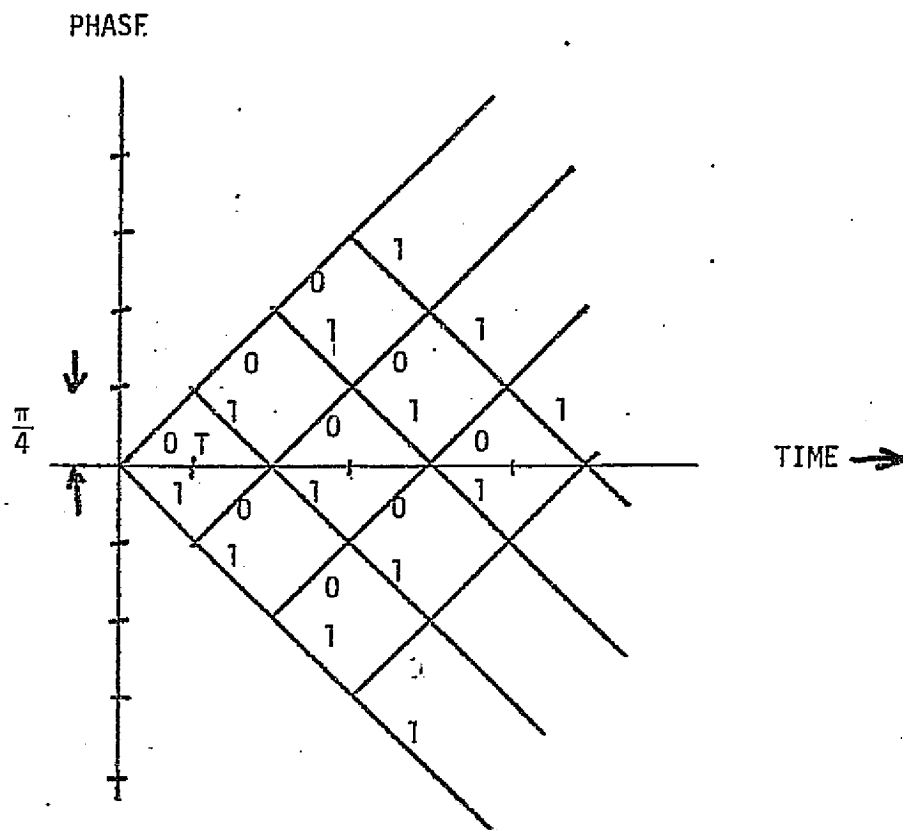
Figure 3-2. Signal Space Representation of KQPSK Signals.
Note that the signal vector transition is
limited to the two possibilities indicated.

Figure 3-3. <u>PHASE TRELLIS REPRESENTATION</u>

<u>OF MOTOROLA MSK/2 (OLD VERSION)</u>

- $m = 2$

- $h = 1/4$

- $\theta(t) = \theta(kT) + d_{kH} \cdot \pi h(t-kT)$

    $kT \leq t \leq (k+1)T$

- $d_k = \pm 1$ (m levels)
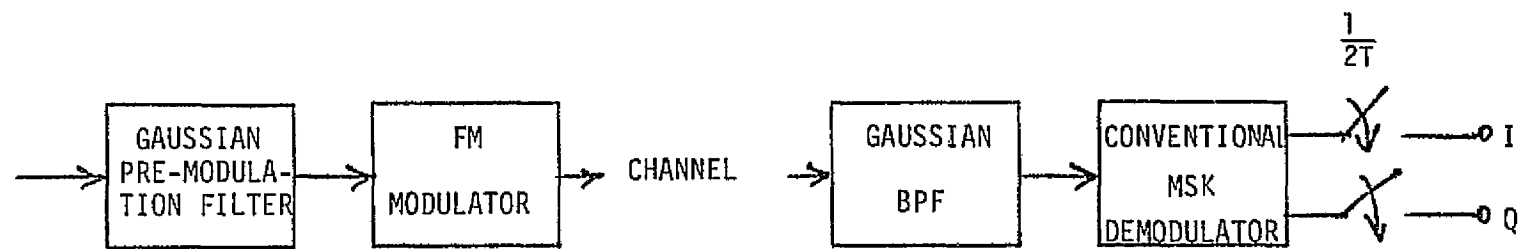
Figure 3-4.   Generation and Demodulation of GMSK Signal.
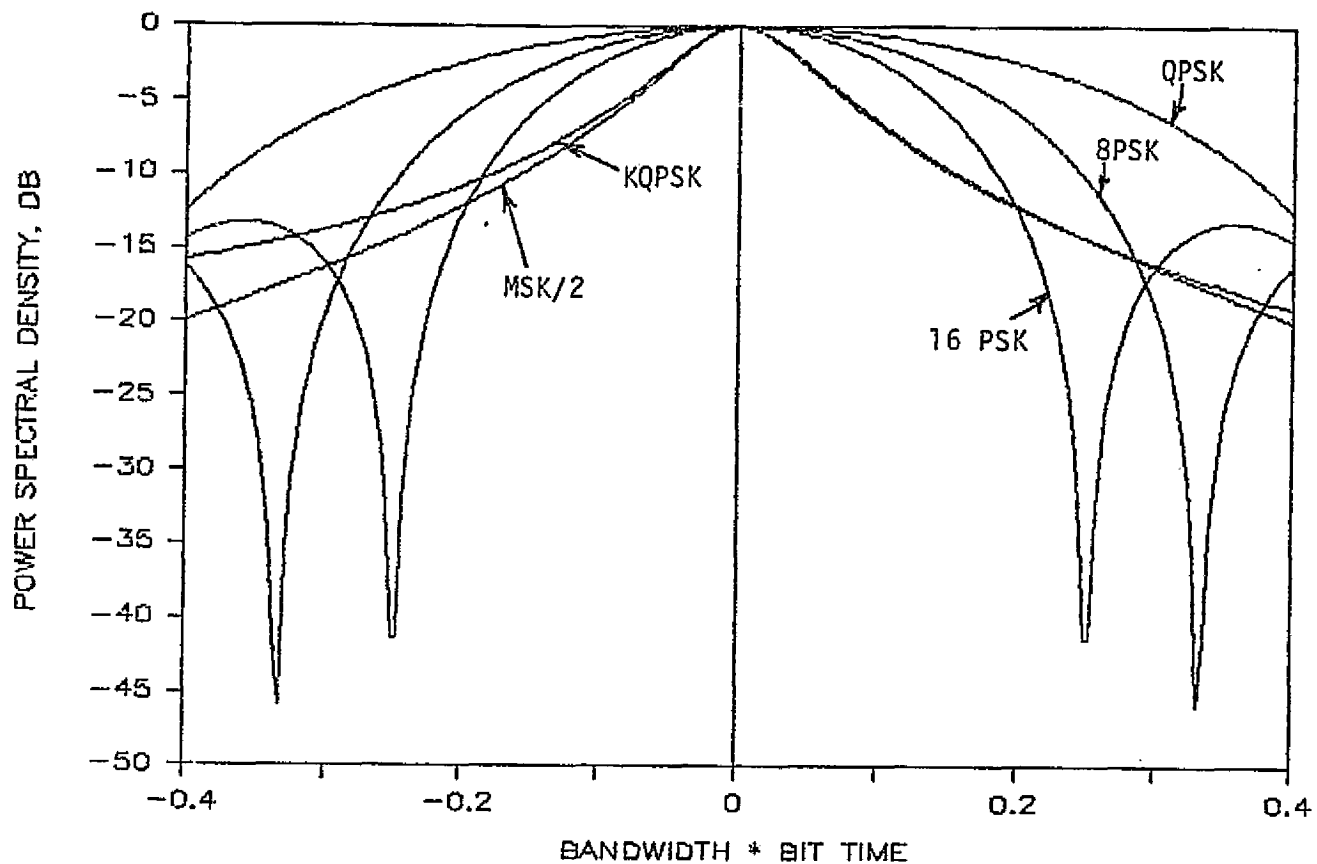
POWER SPECTRUM

Figure 3-5. Power Spectra Comparison.

formats are shown in Figure 3-6. Assuming rate 3/4 coding is employed, the top three contenders are KQPSK, 16PSK, and MSK/2, in terms of spectrum efficiency. However, this is not the only consideration in modulation selection since the degradation from ideal antipodal detection (BPSK) must be considered.

3.3 Simulated Performance

Bit error rate performance for candidate SDT modulation schemes are summarized in Table 3.1 for 85 Mbps data at 15.5 dB E_b/N_0 through a 34 MHz linear channel modeled by a 4-pole Butterworth filter. The detection algorithms are, in most cases, based on sampling a LPF version of the signal (thus duplicating typical hardware implementation). No attempt has been made to optimize the filter types and bandwidths. The modulation schemes are also compared in Table 3.2 when rate 7/8 coding is applied. The meaning of the terms degradation and system margin in Table 3.1 and 3.2 need clarification. Since only the performance of the modulation at 15.5 dB is simulated, the degradation and margin shown are not with respect to a 10^{-7} BER. Instead, the interpretations in Figure 3-7 are adopted. The degradation is really the conventional degradation at, in this particular case, 1.4×10^{-5}. The margin is defined to be the difference between the degradation and the idealized system design margin ($15.5 - 11.5 = 4$ dB). This table is useful only for ranking the simulated performance of various modulations.

Based on Table 3.2, it is determined that 8PSK is the prime candidate for modulation performance evaluation. Since the Motorola MSK/2 modem (SMSK/2, where S denotes serial implementation) did not perform well, Motorola has abandoned this scheme and introduced another SMSK/2 for the SDT purpose. Since the new Motorola SMSK/2 is an
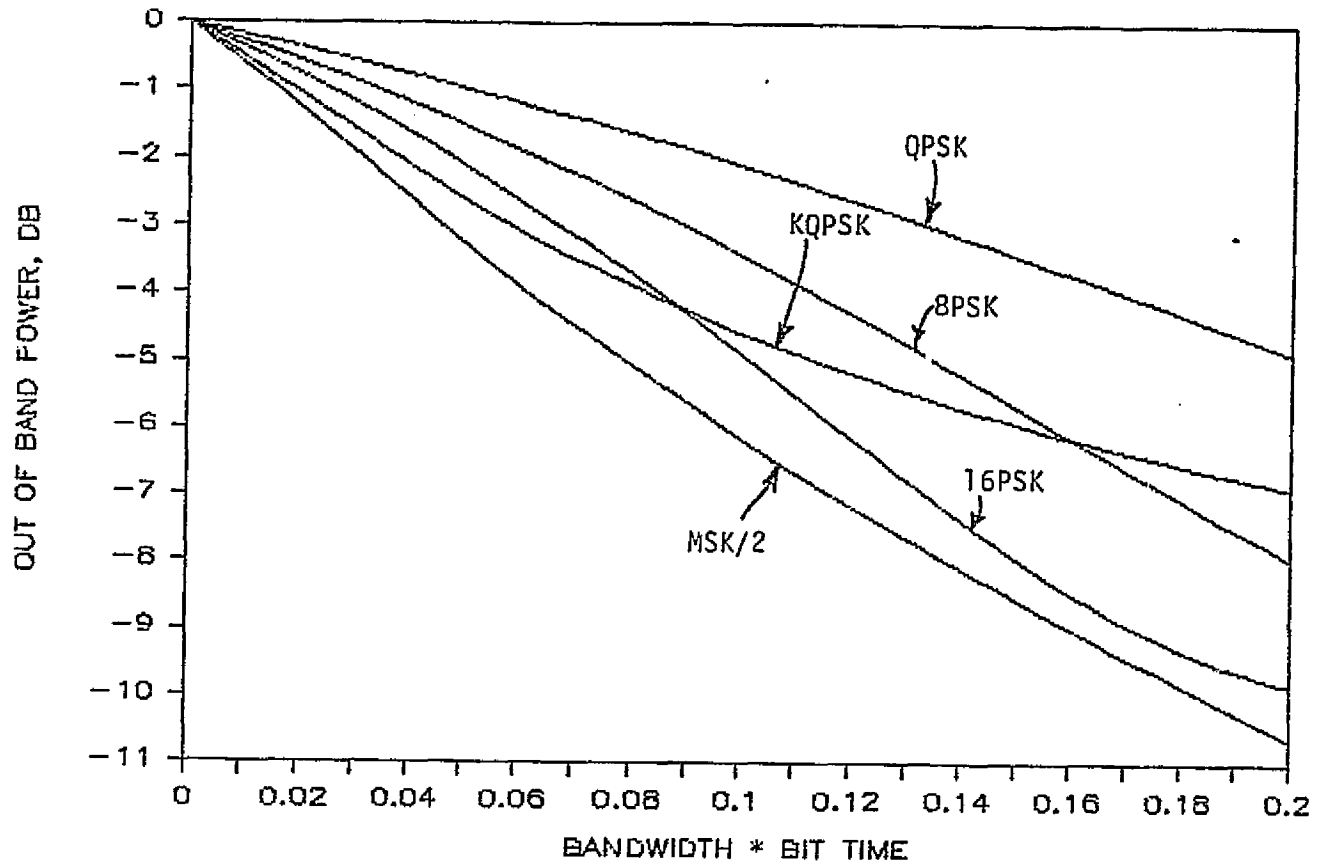
OUT OF BAND POWER

Figure 3-6. Out-of-Band Power Comparison.

Table 3-1.   Candidate SDT Modulation Schemes.

MODULATION SCHEME	DEGRADATION, dB (Rel to 15.5dB)	MARGIN, dB
QPSK	6.1	-1.9
8PSK	4.8	-0.6
16PSK	9.2	-5.0
MSK/2	6.7	-2.5
KQPSK	5.5	-1.3
GMSK	6.7	-2.5

• E_b/N_0 = 15.5 dB

• Data Rate = 85 Mbps

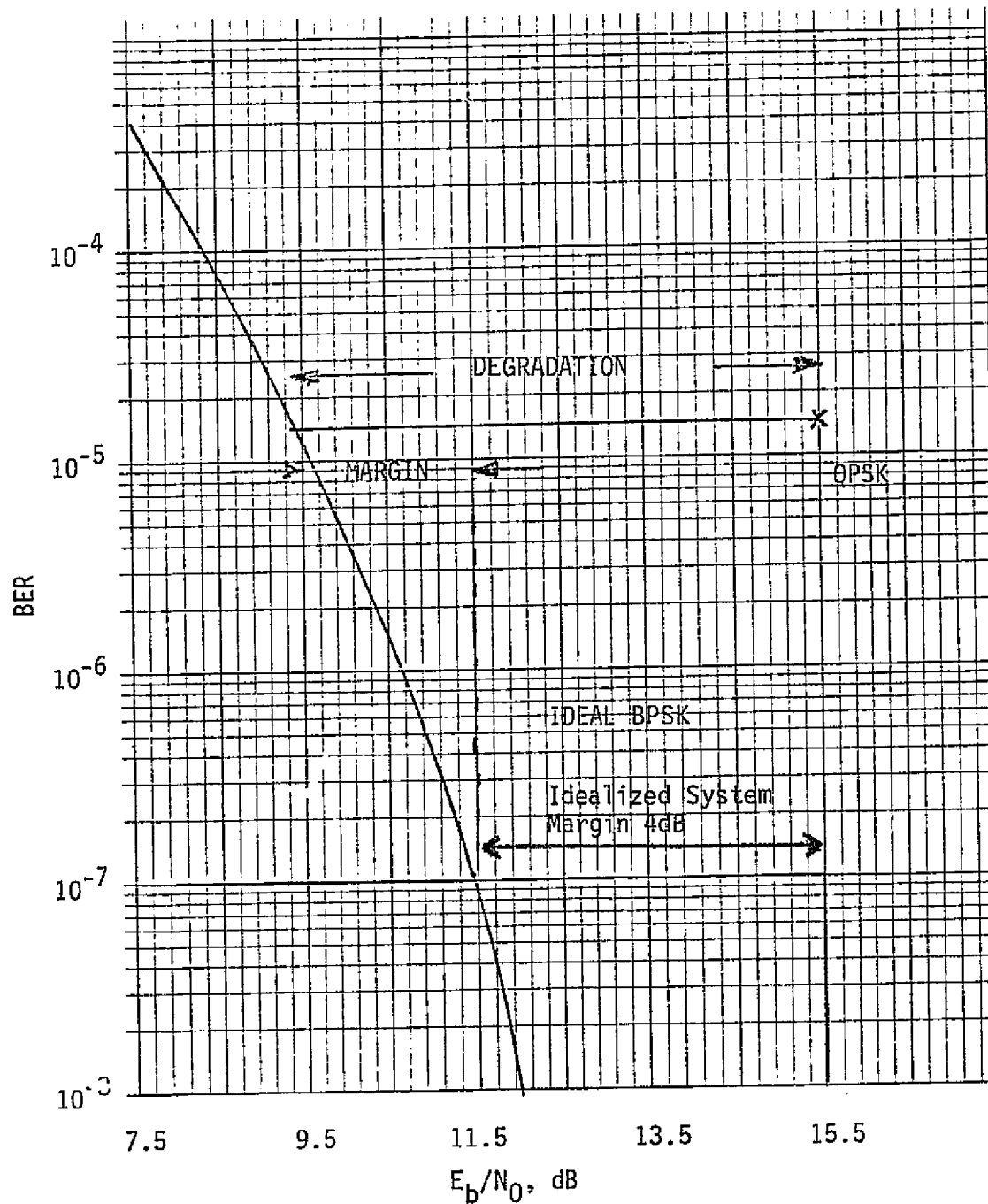• Channel Filter = 34 MHz (4-Pole Butterworth, 3dB BW)

Table 3-2. Candidate SDT Modulation Schemes with
            Coding (Rate 7/8).

MODULATION SCHEME	DEGRADATION, dB (Rel. to 10^{-7})	MARGIN, dB
QPSK	9.6	-5.4
8PSK	6.1	-1.9
16 PSK	9.7	-5.5
MSK/2	9.1	-4.9
KQPSK	6.4	-2.2
GMSK	9.2	-5.0

- E_b/N_0 = 14.9 dB

- Data Rate = 97.14 Mbps

- Channel Filter = 34 MHz

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Figure 3-7. SAMPLE LINEAR CHANNEL PERFORMANCE FOR QPSK

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unconventional modulation scheme, a simplified analytical description of the modulation and demodulation process is given in Appendix I. The Motorola SMSK/2 is more commonly known in the literature as the Duobinary Linear Phase (DBLP) continuous phase modulation. The performance of the new SMSK/2 is approximately 3.2 dB better than 8PSK at a 10^{-4} SER.

Motorola has studied extensively the implementation aspects of the SMSK/2 modem. They have also made a study of the expected hardware losses and compared with 8PSK.The details are included in Appendix II. The main conclusion is that both 8PSK and SMSK/2 modem designs have similar bit error rate performance in an optimized system. However, the SMSK/2 is more tolerant to realistic hardware constraints and is therefore recommended by Motorola.

3.4 Simulation of 8PSK and SMSK/2 Performance Through the SDT Channel

Based on the previous discussion, the 8PSK and the Motorola SMSK/2 are the two prime condidates for the SDT. The modulator and demodulator are modeled for the two schemes and their performances are evaluated with the simulated SDT transmission path as shown in Figure 3-8. The transmission path model has incorporated the most up to date RCA inputs. Figure 3-9 shows simulated performance of the 8PSK modem. Notice that the demodulator must be equalized to achieve 10^{-4} symbol error rate performance. The curves flatten out at a C/N_0 of about 94 dB-HZ. This is due to the fact that although the downlink power is increased by operating the satellite SSPA beyond the nominal point (i.e. 0 dB reference in Figure 2-5), the AM/PM becomes worse. Since the 8PSK is sensitive to phase jitter induced by the worsening AM/PM, the performance improvement achieved by increasing the downlink power is
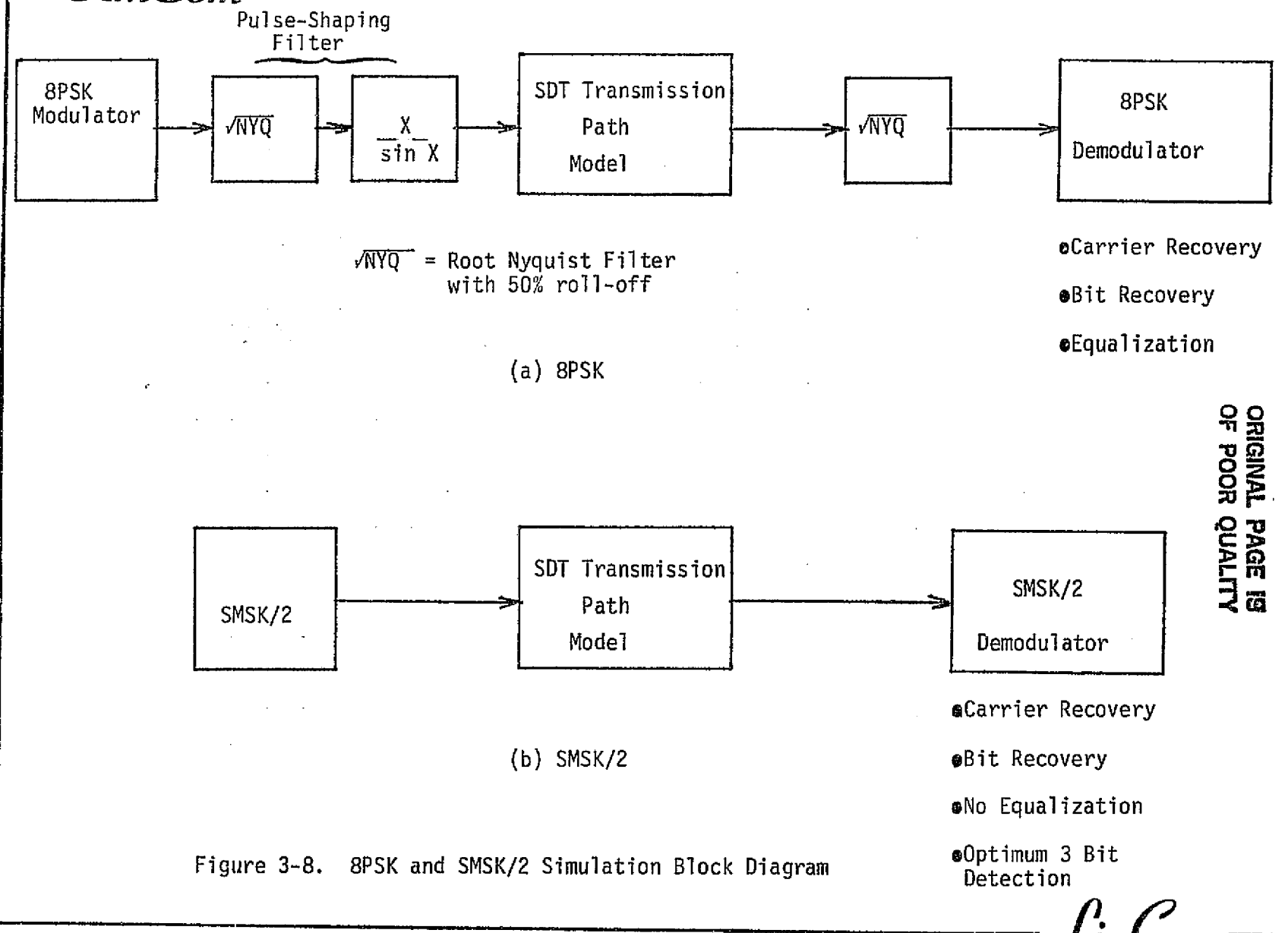
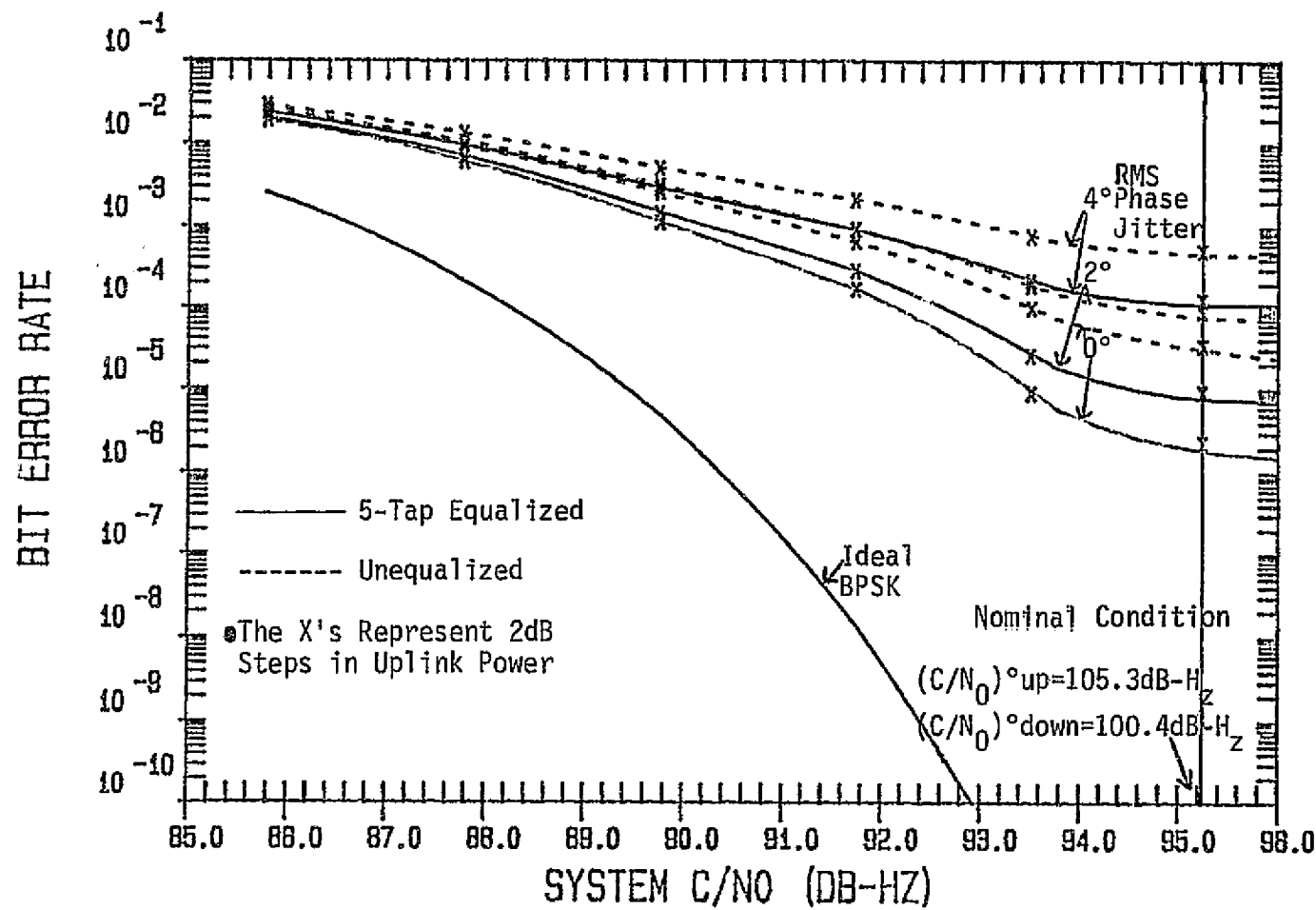Figure 3-8.   8PSK and SMSK/2 Simulation Block Diagram

Figure 3-9.   Simulated Performance of 8PSK at 97.1 Msps (85 Mbps with rate 7/8 Coding)

balanced out by the increase in phase jitter. Therefore the curves flatten out.
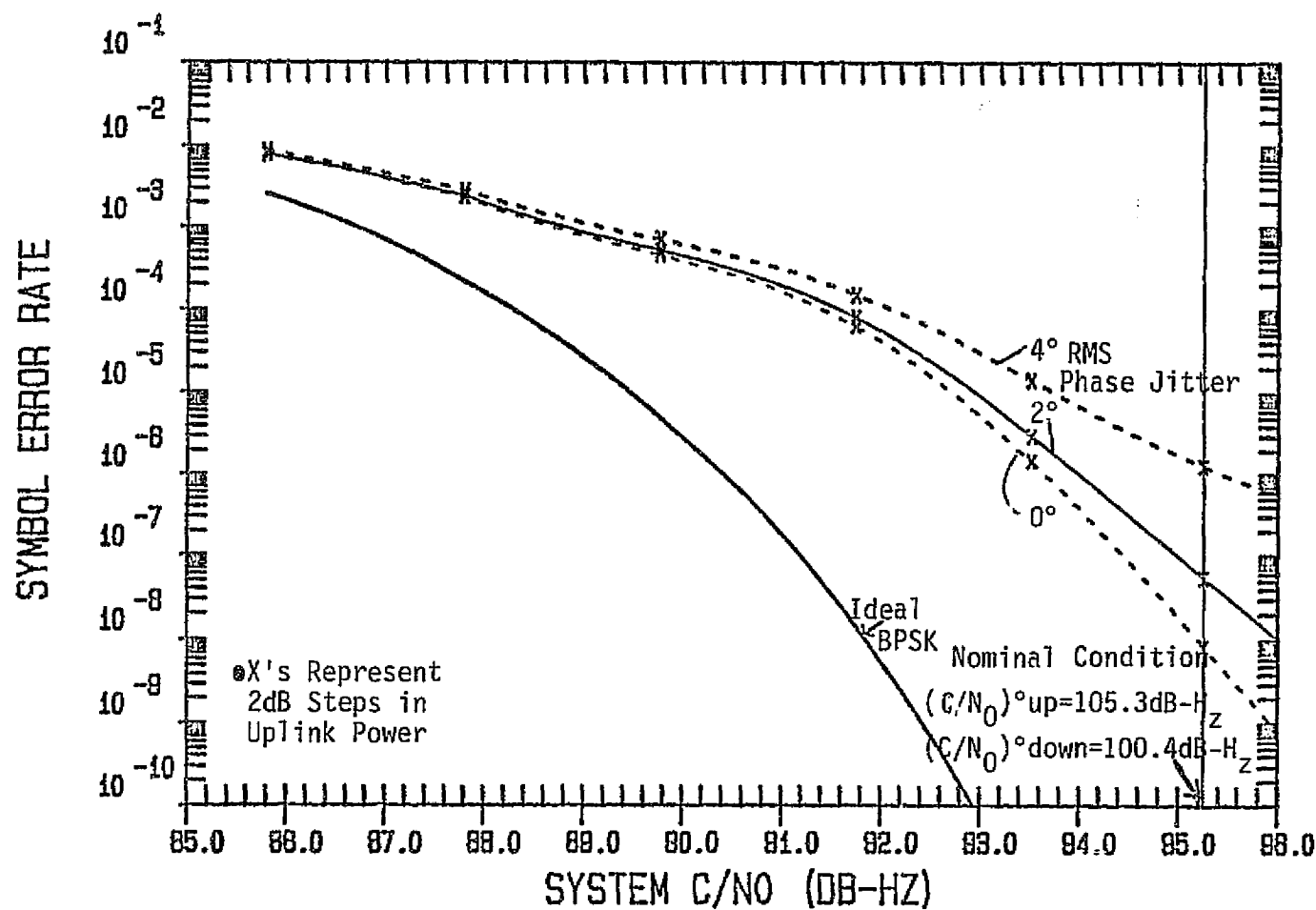
Figure 3-10 shows the simulated performance of SMSK/2 assuming optimum correlation detection by observing 3 consecutive bits. (Appendix I and II assume another form of detection; however, both should yield similar performance at 10^{-4}). Notice that adaptive equalization is not used with SMSK/2. Since the SMSK/2 is rather insensitive to phase jitters, it can be observed that the symbol error rate can be further reduced when the SSPA is operating beyond the nominal point. Table 3.3 summarizes the simulated performances of 8PSK and SMSK/2 (DBLP).

The amount of spectral energy that lies beyond the allocated 34 MHz bandwidth will act as interference to other adjacent user channels of the satellite. There is an RCA out-of-band spectral energy requirement "to keep the spectral energy at frequencies greater than 1.3 times the symbol rate (in Hz), at least 30 dB below the energy referenced to the center frequency of the modulated wideband carrier." Figure 3-11 compares the amount of power outside a fixed bandwidth for the 8PSK and SMSK/2 modulations at the output of the earth terminal HPA output filter.

4.0 Coding Selection

Forward error correction (FEC) must be employed to provide the extra margin to meet the SDT BER performance. Coding performance is often given in terms of coding gains in additive white Gaussian noise channel. The measure is also applicable to the SDT channel if the coding gain is used in the context of Figure 4-1 relating channel symbol error rate (SER) to decoded system bit error rate (BER). For example,

$\mathcal{L}in\mathcal{C}om$

Figure 3-10.   Simulated Performance of SMSK/2 at 97.1 Msps (85 Mbps with rate 7/8 coding)

$\mathcal{L}in\mathcal{C}om$

Table 3-3.   Performance Summary

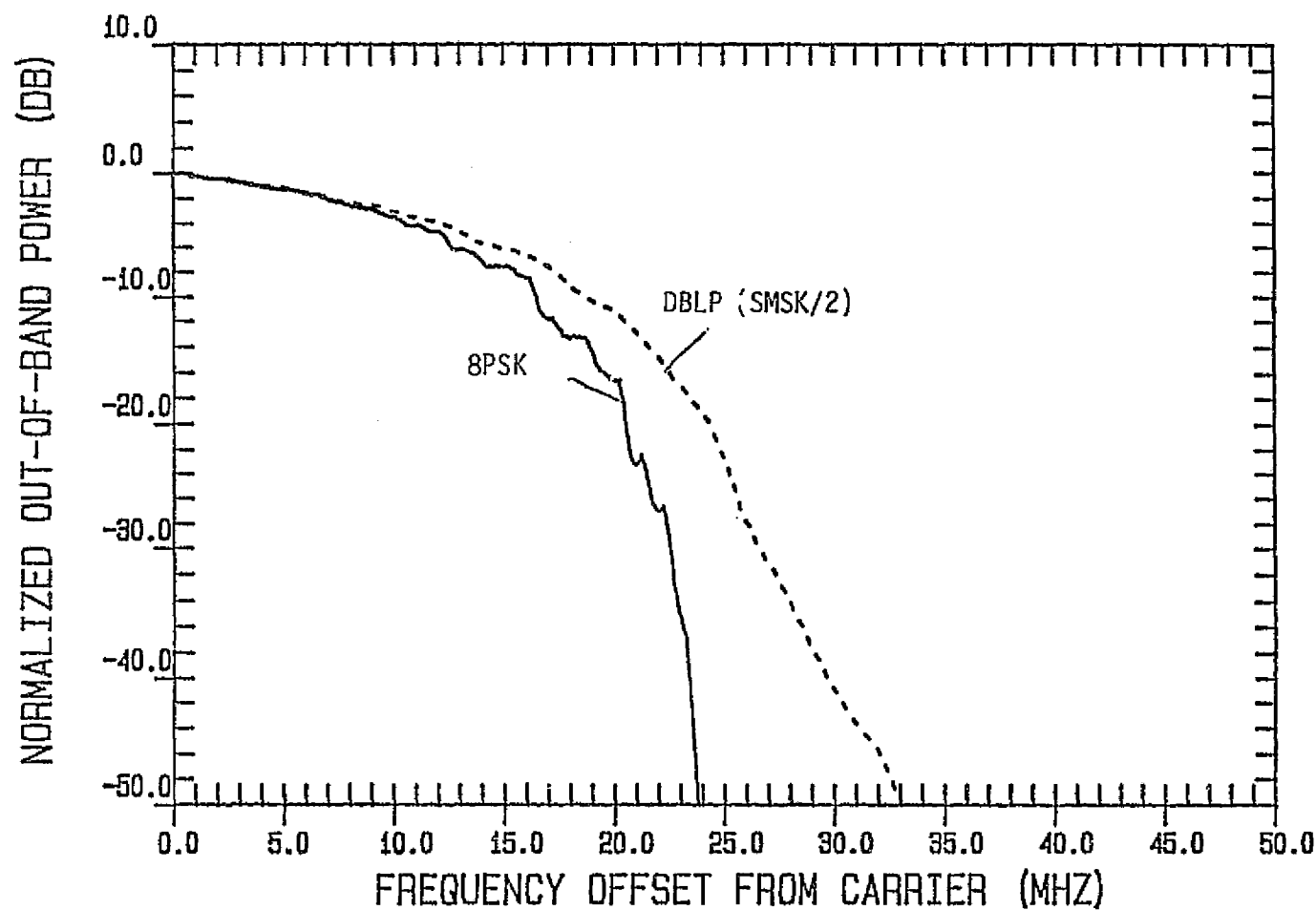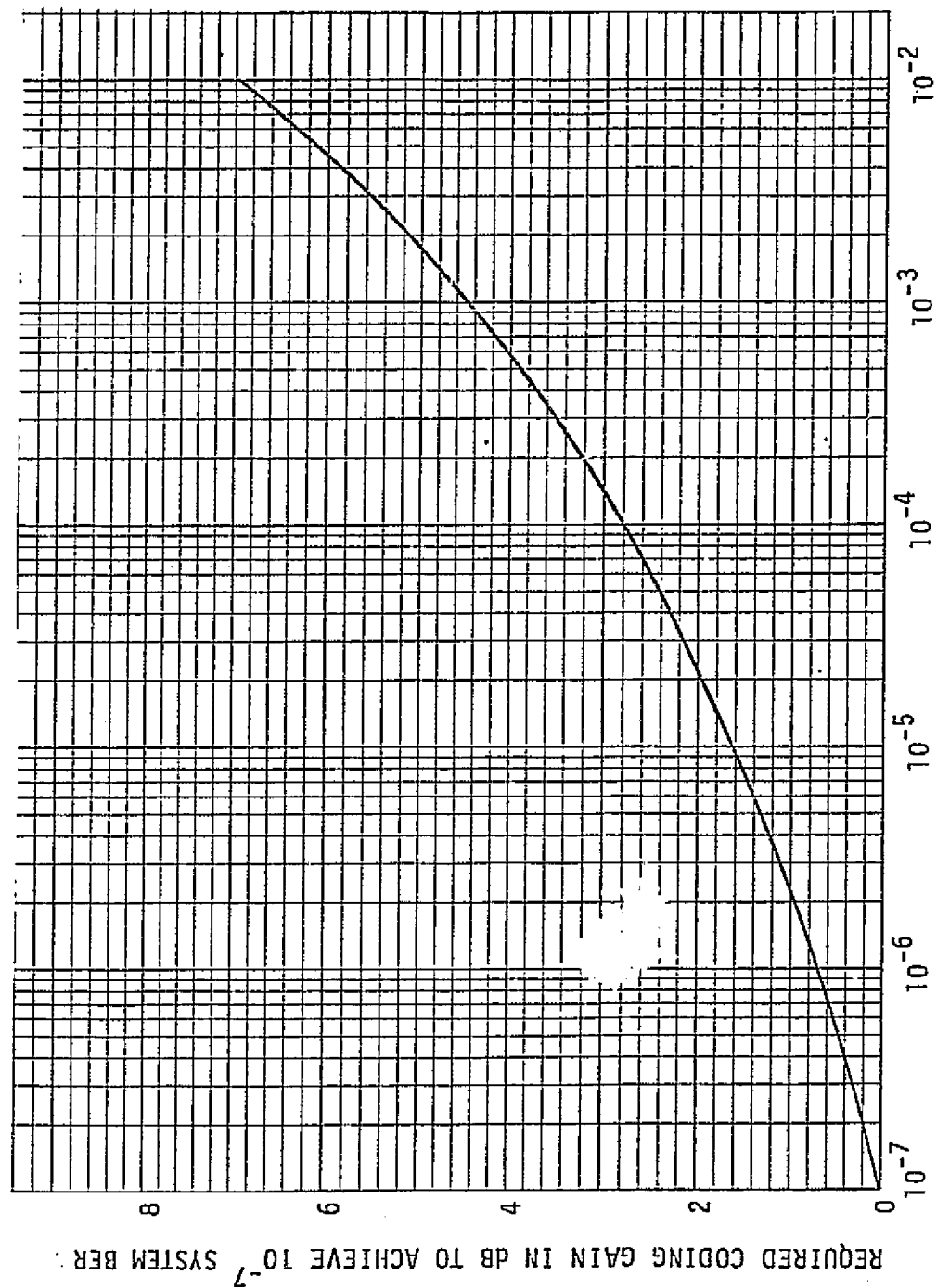| Conditions	Margin At 10^{-4},dB		
	8PSK		SMSK/2
	Unequalized	Equalized	
No Phase Jitter	0.0	3.0	3.8
2° RMS Phase Jitter	NA	2.6	3.6
4° RMS Phase Jitter	NA	NA	3.2

Figure 3-11. Out of Band Power Comparison

Figure 4-1. Required Coding Gain vs Channel Symbol Error Rate

-44-

if the channel SER is 10^{-4}, then a coding gain of 2.8 dB is required to achieve a decoded system BER of 10^{-7}. From the previous sections, the 10^{-4} SER is a realistic target, so that coding techniques that provide 3 to 5 dB coding gains are required. Because of the bandwidth expansion associated with coding, the coding rate must be limited to between 3/4 and 7/8. Table 4.1 summarizes some practical coding schemes that can potentially meet the SDT coding gain and code rate requirements. The first two convolutional codecs (Viterbi decoding, sequential decoding) are commercially available. The third convolutional codecs has been used extensively in satellite links and is used in the existing 50 Mbps modem. The algerbraic codes have low complexity. Table 4.2 lists some applicable algerbraic codes and Figure 4-2 shows a typical decoder.

In summary, the two prime candidates for coding for SDT are the convolutional codes using sequential and threshold decoding. The tradeoffs are complexity, cost and performance. These issues will be addressed in a later section.

5.0 Technology Assessment

5.1 Modem

5.1.1 SMSK/2

The Motorola SMSK/2 modem builds upon the serial MSK (SMSK) modem that Motorola has developed under contract to NASA Lewis Research Center for the "30/20 GHz Communications Systems Baseband Processor Subsystem." The SMSK modem has been constructed and tested for 750 Kbps and 760 Mbps [1,2]. At 760 Mbps, the measured back-to-back performance degradation is about 1.3 dB. At 95 Mbps, the degradation can be expected to be smaller (around 0.5 dB).

The proposed SMSK/2 modem basically uses the same demodulator.

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Table 4-1.   <u>COMPARISON OF APPLICABLE CODING SCHEMES</u>

CODEC	CODING GAIN	COMPLEXITY
CONVOLUTIONAL CODES		
• VITERBI DECODING	4.6 dB	High
• SEQUENTIAL DECODING	4.9 dB	High
• THRESHOLD DECODING	3.7 dB	Medium
ALGEBRAIC CODES	2.5 dB	Low

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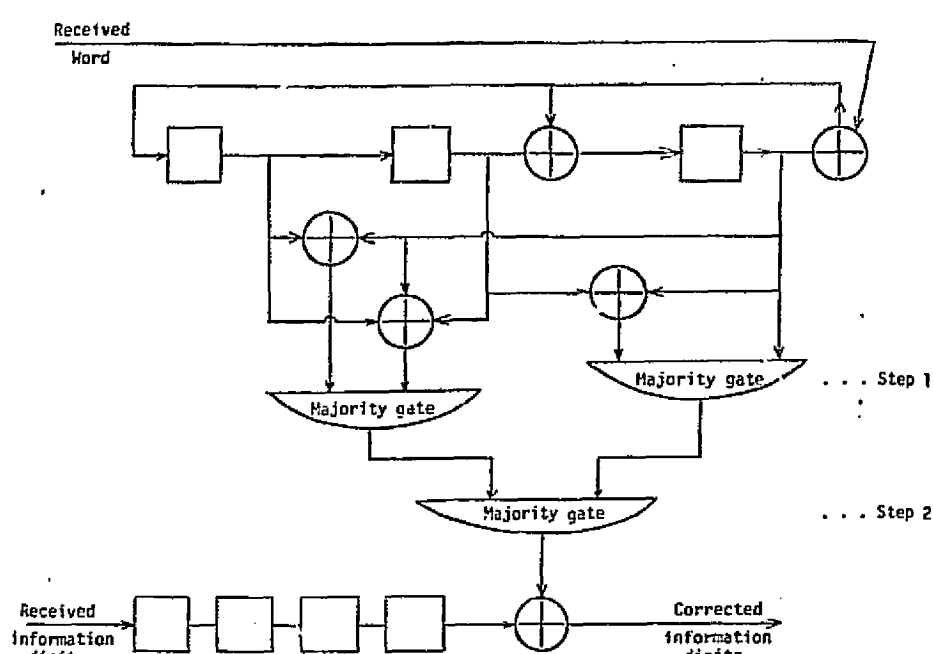Table 4-2.   <u>APPLICABLE BINARY EUCLIDEAN GEOMETRY</u>
<u>CYCLIC CODES</u>

WORD LENGTH (BITS)	INFORMATION BITS	CODE RATE	CODING GAIN (dB)
15	11	0.73	1.7
31	26	0.84	2.2
63	57	0.905	2.5
63	48	0.76	3.6

• RATE 7/8 = .88

• RATE 3/4 = .75

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Figure 4-2. **A TWO-STEP MAJORITY-LOGIC DECODER FOR THE (7,4) BINARY CYCLIC HAMMING CODE**

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However, the modulator section is rather different, see Appendix II. It appears the risk there is the ability to specify and procure filters in the modulator that can yield the required performance.

The satellite channel is also unique in the sense of involving nonlinearities and narrowband filtering. Certainly, the SMSK/2 modem has not been tested for this application. However, judging from its relative insensitivity to carrier phase jitters and bit sync timing errors, the SMSK/2 modem should be acceptable.

It was shown earlier in the simulation results that the 8PSK modem requires some sort of equalization in order to provide any system margin. The performance of SMSK/2 was simulated without such equalization and still showed better performance than 8PSK. It is anticipated equalization may provide some further margin, although not as significant as for 8PSK. In terms of implementation, Motorola does not think that the 5-tap delay line equalizer design is a major effort.

5.1.2 8PSK

The 8-phase PSK modulation is a well established technique for common carrier transmission of high speed data (up to 90 Mbps) streams over microwave facilities since the late 70's [3-10]. The 8PSK modulation has been used to transmit two DS3 data streams (90 Mb/s) in a 30 MHz RF bandwidth. This is 3 bits/sec/Hz and is close to the SDT application of 2.86 bits/sec/Hz (97 Mb/s over 34 MHz). Because of the close agreement between bandwidth and data rate, it is expected that the microwave radio type of modulator and demodulator design can be carried over directly to the SDT.

The back-to-back modem loss for the microwave system is typically in the order of 2.5 dB and includes a 1.0 dB loss due to the pulse

...

shaping filters and a 0.3 dB loss due to differential encoding.

The 8PSK modulation has not found much use for the satellite channel except for experimental purposes [11]. This is perhaps due to the relatively large loss of 8PSK relative to QPSK, the predominant modulation technique for satellite applications. In this sense, the 8PSK SDT application may be considered a prototype project by most vendors, which requires R & D effort.
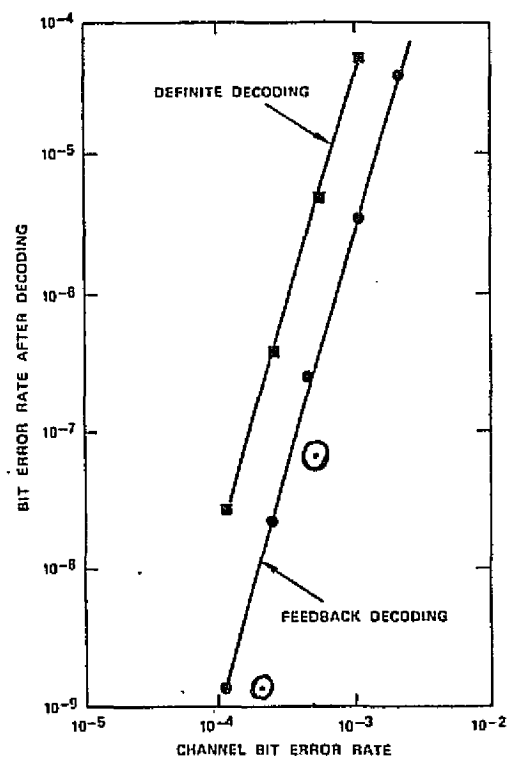
5.2 Coding

5.2.1 Threshold Decodable Convolutional Codes

The threshold decodable convolutional codes have been used extensively in satellite links. They are also used in the existing 50 Mbps modem/codec. The measured performance of the 50 Mbps modem/codec, shown in Figure 5-1, agrees closely with the theoretical performance using feedback decoding. Appendix III documents Motorola's assessment on the implementation of this codec. The codec does not represent any technical risk and is not expected to be a cost item. However, the performance is about 2 dB worse than the sequentially decoded convolutional code to be addressed next.

5.2.2 Sequentially Decoded Convolutional Codes

Commercially available rate 7/8 convolutional codecs employing sequential decoding (e.g. Linkabit LS2017) can provide up to 4.9 dB gain at 10^{-7} decoded bit error rate. However, the codec can only operate with data rates less than 12 Mbps. For this reason, individual codecs must be multiplexed together. For 85 Mbps, 8 codecs are required as shown in Figure 5-2. This multiplexing scheme is used for the TDRSS Ku-band and Shuttle unique equipment. The cost of implementing this multiplexed system for convolutional codes must be weighed against the

Figure 5-1.   MEASURED ERROR RATE OF THE DITEC CODEC

⊙ RCA MEASUREMENT DATA FOR

50 Mbps MODEM

CE = Convolutional Encoder

CD = Convolutional Decoder
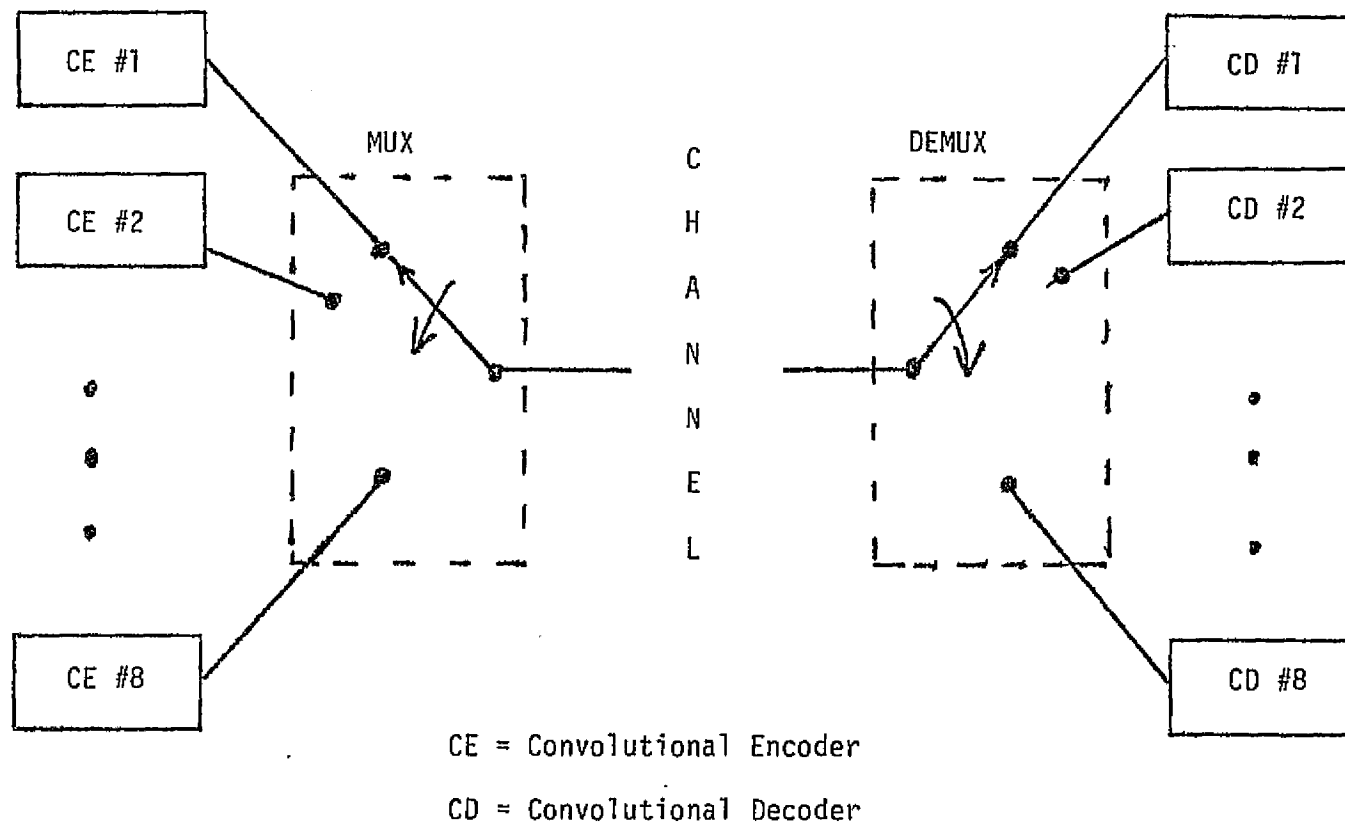
Figure 5-2. Multiplexed Convolutional Codes.

improvement in coding gain when comparing with threshold decodable codes. According to Elie Levy of M/A-com Linkabit, the LS2017 codec is currently implementated with TTL logic. If it is instead implemented with ECL logic, the data rate can be increased from 12 to 50 Mbps so that the number of building block codecs in Figure 5-2 can be reduced from 8 to 2. This can be a cost trade-off consideration.

5.2.3 Punctured Convolutional Codes for Viterbi Decoding

Harris had developed a 5Mb/s rate 1/2 convolution encoder/Viterbi decoder chip under their VHSIC program. A copy of the Harris preliminary specification is provided by J. S. Reese of Harris and is shown in Figure 5-3. The 85 MB rate 7/8 coder can be configured with rate 1/2 VHSIC Viterbi codecs by adding data multiplexers, supporting logic and RAM memory, using the so-called punctured coding technique [12,13]. The coding gain at 10^{-7} is about 3.8 dB [13] and is comparable with the threshold decodable convolutional codes.

6.0 Cost Assessment

Aside from Motorola, a number of vendors were polled regarding their interest in developing the modem/codec and a rough cost estimate on the equipment. Table 6.1 is a summary of such a survey.

The cost assessment here is based on two full duplex units.

6.1 Modem

6.1.1 SMSK/2

The estimated man years for the Motorola SMSK/2 modem is 15.3 man years, equating to a ROM price of $2,000,000. This also includes the price of the codecs for threshold decodable convolutional code. The detailed cost and schedule breakdown is given in Appendix IV. It is estimated that the codec cost included is approximately $200,000.

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Modem Engineering
J.S. Reese, Section Head
(305) 727-4067

Figure 5-3. VLSI/VHSIC K=7 VITERBI CODEC
PRELIMINARY SPECIFICATIONS

Data Rate	Up to 5Mb/s bit rate (10 Mb/s symbol rate)*
Performance	4.9 dB coding gain at 10^{-5} BER
Coding Polynomial	Rate 1/2, CL-7
Acquisition Time	TBD
Mean Time to Loss of Lock	TBD
Operating Modes	QPSK (dual input), BPSK (single input), both in continuous or burst mode (minimum 16 bit burst), with synchronous or asynchronous clocks (bit rate and trace-back clocks)
Input Data Formats	3 bits for each coded pair in either sign/ magnitude or offset/binary, NRZ-L, -M, -S
Output Data Format	NRZ-L
Input Data/Clock Relationship	Accepts data changes at rising edge of clock
Output Data/Clock Relationship	Data changes at rising edge of clock; two output clocks available: one follows bit synchronization changes for true delay, the other is fixed for cripto data purposes
Branch Synchronization	Resolves swapped Ra & Rb coded pair for either QPSK or BPSK modes, plus swapped and staggered QPSK coded pair; accepts inverted/ non-inverted Rb coded symbols
Throughput Delay	76 bits worst case (QPSK staggered)
Output Status	Lock, signal quality (4 Bits)
Testability	LSSD
IC Voltages	VDD = 3.3 ± 0.3 V, Ground
Interface	Low power schottky TTL with pull ups to chip's VDD (3.3 V)
Power Consumption	Less than 1/4 watts
Size	85 pins (package TBD)
Operating Temperature	-55° C to +125°C
Rate 1/2, CL-7 Encoder	Included in chip with all features to match decoder

*Under total worst case conditions

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Vendor	Contact	Equipment	Comments
M/ACOM - DCC	Tom Stilwell (301) 428-5500	8PSK Modem	500 - 1M
Comsat Lab	Chester Wolejsza (301) 428-4255	8PSK Modem	600K, Parallel in House RND
		Rate 7/8 Threshold Codec	240K
Aydin Monitor	Bob Clegg (215) 646-8100	8PSK Modem	1M, Relatively High Risk
Raytheon Telco	Gene Hunt (617) 769-7510	8PSK Modem	Discontinued Product Line
NEC	Mr. Iida (703) 560-2010 (x302)	8PSK Modem	Not Interested in R & D Prototype
Rockwell Collins	John Beckerich (214) 996-7676	8PSK Modem	Not Interested. Product is for direct 6 GHz Mod/Demod for terrestrial microwave link operations.
M/ACOM-Linkabit	Elie Levie (619) 457-2340	Codec	500K
Harris	J.S. Reese (305) 727-4067	Codec	Competitive

Table 6.1. Vendor Survey

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6.1.2 8PSK

It is interesting to note that all the terrestrial microwave link equipment manufacturers (NEC, Rockwell Collins, Raytheon) are not interested. Of the interested vendors, Aydin Monitor's estimate is $1,000,000 and they consider the program will be relatively high risk. M/A-com DCC's estimate is between $500,000 to $1,000,000. The most interested vendor is COMSAT Labs since they are currently developing a 210 Mbps 8PSK TDMA modem under in-house R&D funds and have spent over $500,000. Assuming the procurement is one year from now so that they can take advantage of their in-house program, their estimate is $600,000 of which $450,000 is labor and $150,000 is parts.

6.2 Codec

The ROM price from Linkabit for the rate 7/8 sequential decoded convolutional codecs is $500,000. This includes 16 LS2017 codec units at $14,000 each and the balance is for the data multiplexers. It is also estimated that the cost of developing ECL implementation will be comparable.

Motorola gave a ROM price of $310,000 for the Viterbi Decoders.

Harris did not give a ROM price but stated that the price will be competitive.

Comsat Labs' estimate on the threshold decodable convolutional codecs is $240,000 which includes $230,000 for labor and $10,000 for parts.

7.0 Analytical Simulation

The analytical simulation adopted by LinCom for the SDT evaluation is described in detail in Appendix V.

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[13] Y. Yasuda, K. Kashiki and Y. Hirata, "High-Rate Punctured Convolutional Codes for Soft Decision Viterbi Decoding", to appear IEEE Trans. Commun.

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APPENDIX I

MOTOROLA SMSK/2 (DBLP)

APPENDIX I

Motorola SMSK/2 Modulator Model

Figure 1 shows an equivalent model of the SMSK/2 modulator. The input ± 1 NRZ data waveform $d(t)$ representing the data sequence {$\cdots d_{-1}$ d_0 $d_1 \cdots$} with bit time T is first converted to a tri-level signal by the operation indicated. The associated waveforms are shown in Figure 2. The signal $\lambda(t) = d(t) + d(t-T)$ is used to control the frequency of the FM modulator output. The frequency deviation of the output is $\pm \frac{1}{2T}$ Hz when $\lambda(t) = \pm 2$ and zero Hz when $\lambda(t) = 0$, or simply

$$\Delta f = \frac{\lambda(t)}{4T} \text{ (Hz)} \tag{1}$$

Mathematically, the output of the FM modulator has the form

$$s(t) = \sqrt{2P} \cos[2\pi f_c t + \theta(t)] \tag{2}$$

where the radian frequency deviation from the carrier frequency f_c is given by

$$\dot{\theta}(t) = \frac{\pi}{2} \sum_{k=-\infty}^{\infty} d_k g(t-kT) \tag{3}$$

The phase process is given by the integral of (3)

$$\theta(t) = \frac{\pi}{2} \sum_{k=-\infty}^{\infty} d_k q(t-kT) \tag{4}$$

with $q(t) = \int_{-\infty}^{\infty} g(t)dt$. The functions $g(t)$ and $q(t)$ are shown in Figure 3. Other continuous modulation schemes [1,2] can be described with (3)
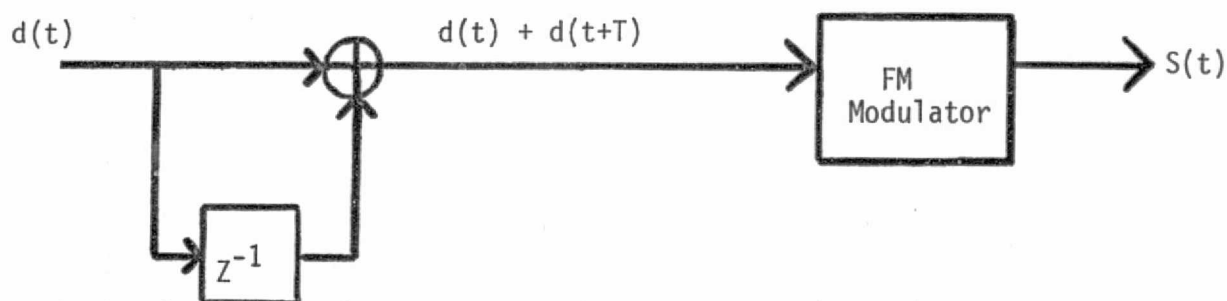
$$S(t) = \sqrt{2P} \ \cos[2\pi_c t + \theta(t)]$$

$$\dot{\theta}(t) = \frac{\pi}{2} \sum_{k=-\infty}^{\infty} \dot{d}_k \ g(t-kT)$$

$$\theta(t) = \frac{\pi}{2} \sum_{k=\infty}^{\infty} d_k \ q(t - kT)$$

Figure 1.   SMSK/2 Modulator Model
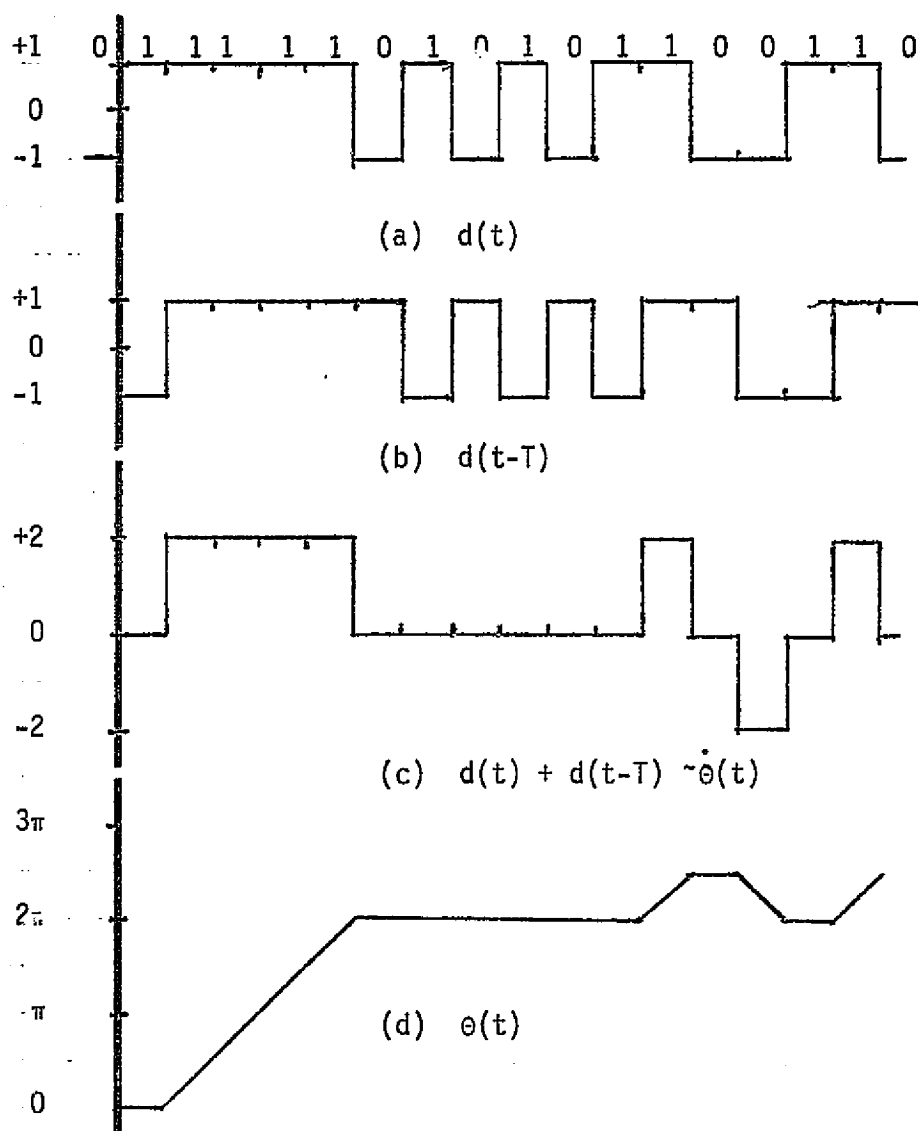
Figure 2.   Waveforms Associated with the SMSK/2
Modulator

g(t)

$\frac{1}{4T}$

0   T   2T

(a) Frequency Pulse

q(t)

$\frac{1}{2}$

0   T   2T
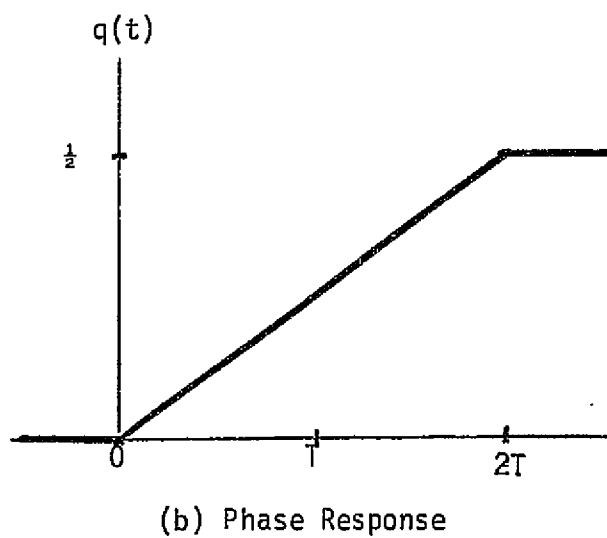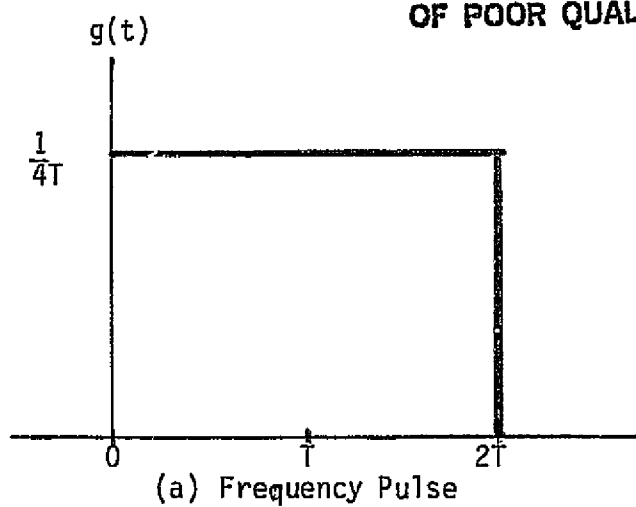
(b) Phase Response

Figure 3.   Frequency Pulse and Phase Response

and (4) when different frequency pulses g(t) are used.

Based on (4), one can readily show that the net increase of the phase $\theta(t)$ at the end points $t = kT$ and $t = (k+1)T$ is given by

$$\theta_{k+1} - \theta_k = \frac{\pi}{4} (d_k + d_{k-1}) \qquad (5)$$

where $\theta_k \triangleq \theta(kT)$. The convention used is that d_k is the data bit between time $t = kT$ and $t = (k+1)T$. Based on (5) and assuming $d_{-1} = -1$ and $\theta_0 = 0$, The phase tree can be traced out for all combinations of data sequence $\{d_k\}$. An example for $0 < t < 4T$ is shown in Figure 4a. One can verify that the data sequence and associated phase trajectory in Figure 2 are in agreement with that of the phase tree.

Motorola SMSK/2 Demodulator

The optimal way to demodulate continuous phase modulation is to examine a duration of NT received waveform, correlate it with 2^N possible phase trajectories and make a decision on the first bit. If one uses a brute force approach, 2^N correlators have to be implemented. This is obviously rather formidable if N is large. A better approach is to use the Viterbi algorithm which reduces the receiver complexity considerably. For SMSK/2, it turns out that using N = 3 yields nearly optimal performance so that only $2^3 = 8$ correlators are required. With such an implementation, the asymptotic degradation (at very low BER) of SMSK/2 relative to ideal BPSK in additive white Gaussian noise enviornment is about 0.7 dB.

Another approach to demodulate SMSK/2 is called serial demodulation and is the one adopted by Motorola. The demodulator is shown in Figure 5. The received signal corrupted by noise, is converted to its I and Q

Figure 4. SMSK/2 Phase Tree
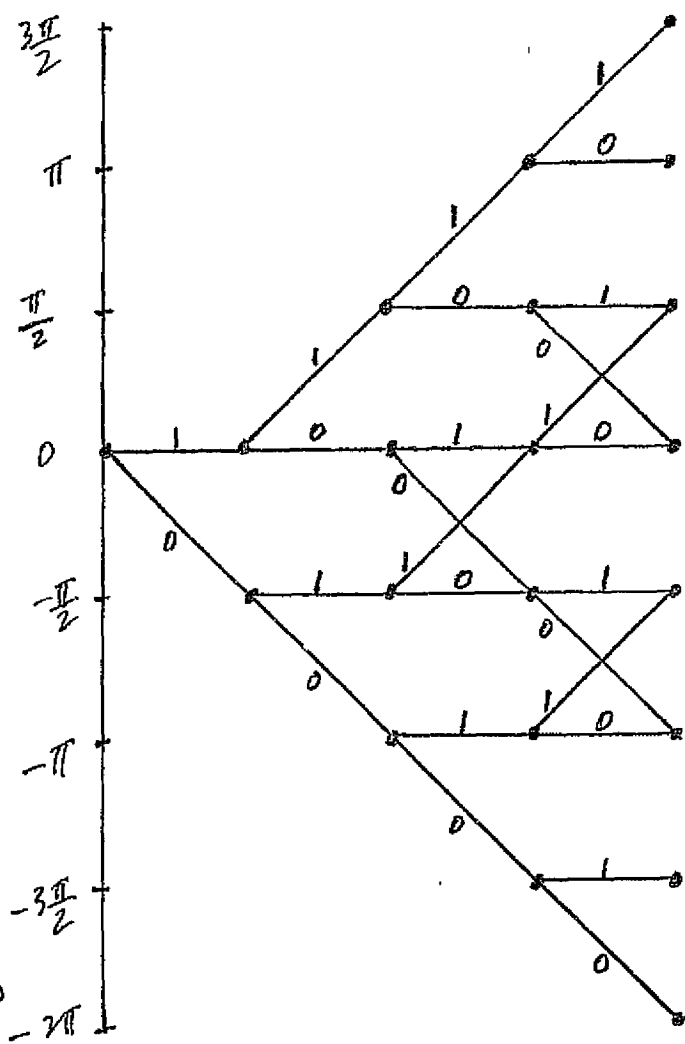
(a) Modulator Output Phase Tree
Zero Assumed for θ_0
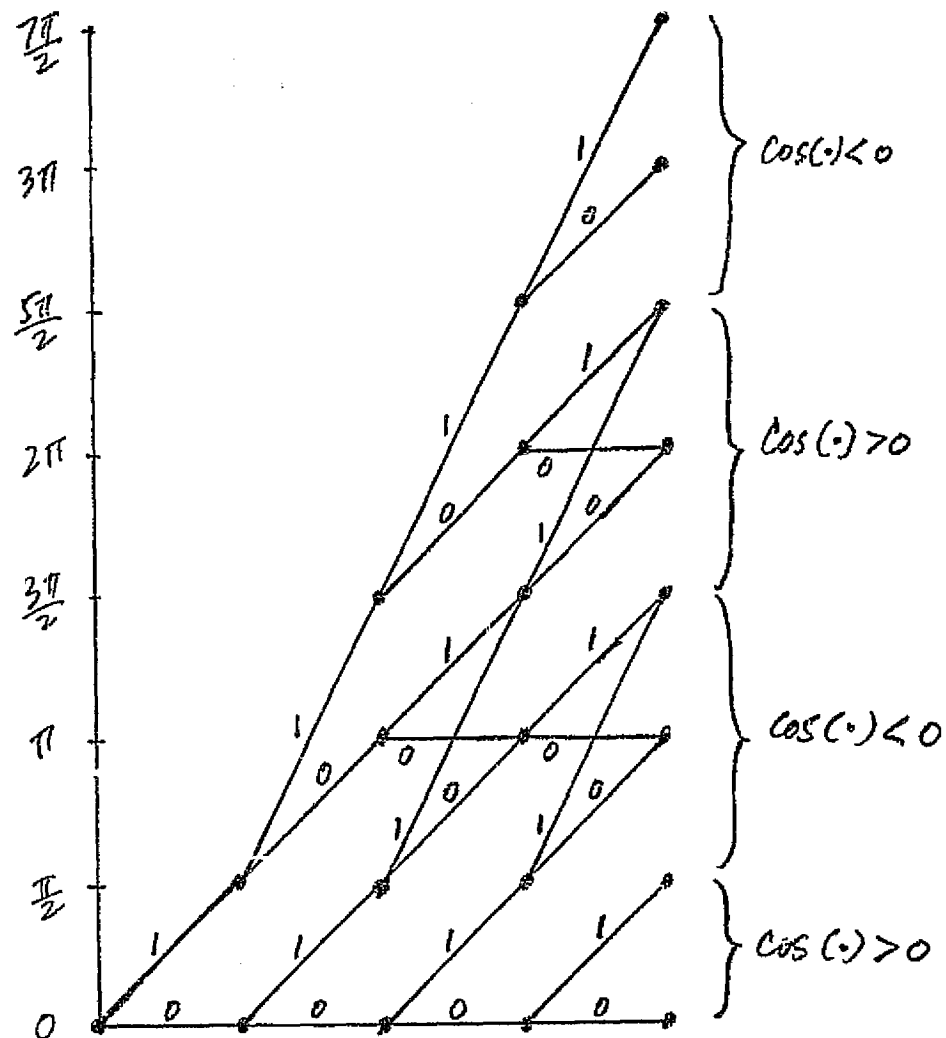
(b) Seriel Demodulator Output Phase
Tree

components by a local reference at $f_c - \frac{1}{4T}$ Hz. Ignoring the double

frequency term, the signal component of the I and Q waveforms are

$\cos[\theta(t)+ \frac{\pi t}{2T} -\phi]$ and $\sin[\theta(t)+ \frac{\pi t}{2T} -\phi]$ where ϕ is the phase error of the

local reference. The phase tree of this demodulated signal is related

to $\theta(t)$ by a constant frequency offset as shown in Fiugre 4b with $\phi =$

0. Notice that the data sequence can be reconstructed in a simple way

by looking at the I component of Figure 5, i.e., the cosine of the phase

tree in Figure 4b. If the previous bit is zero, from Figure 4b it can

be verified that during the next bit period the I component has the same

sign as the previous bit period. If the previous bit is one, then the I

component will have an opposite sign during the next bit period.

Therefore, by observing the sign changes during two consecutive periods,

one can determine the first bit. This algorithm is shown as the last

step in Figure 5.

In the presence of noise, one can filter the received signal to

maximize the signal-to-noise ratio of the detection samples. This is

the function of the filters $h_1(t)$ and $h_2(t)$. In general, the filters

are of the form

$$h_1(t) \;\; = \;\; a(t) \cos \pi t/2T \qquad\qquad (6)$$

$$h_2(t) \;\; = \;\; -a(t) \sin \pi t/2T \qquad\qquad (7)$$

For MSK serial receiver, the optimum waveform of a(t) that achieves

ideal BPSK perfomance is
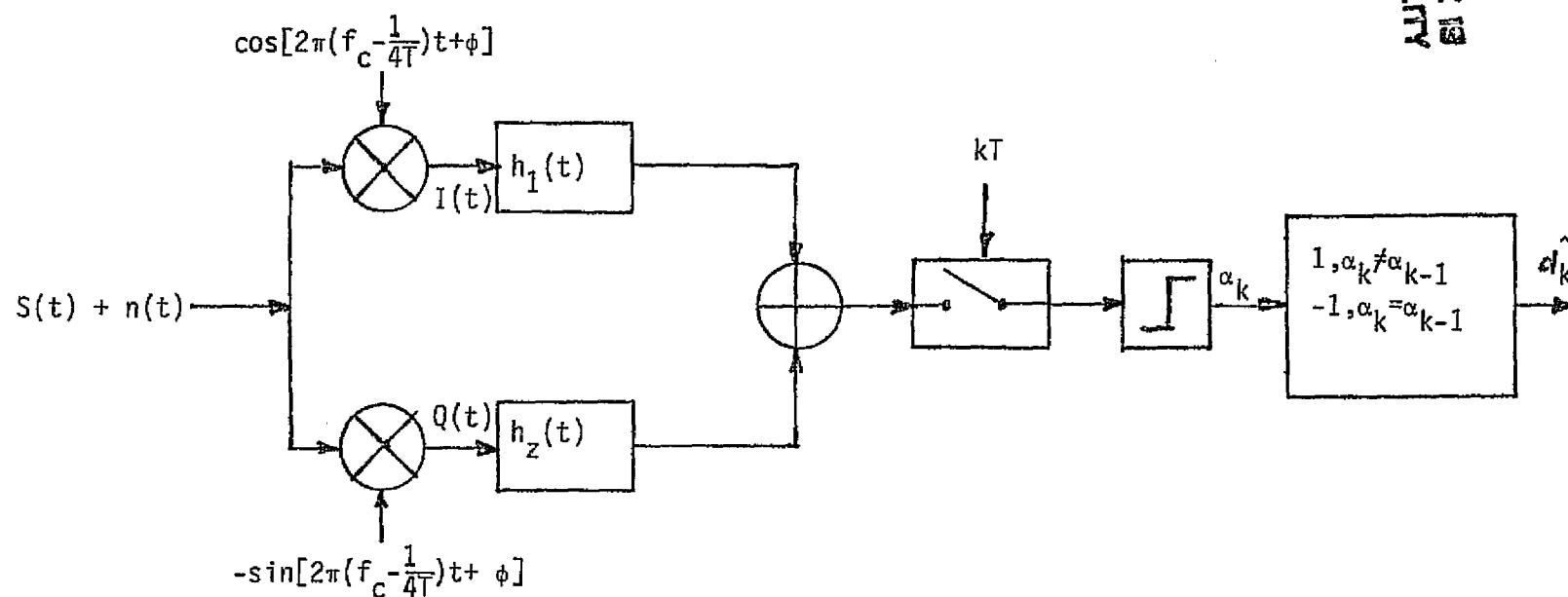
Figure 5. Motorola SMSK/2 Demodulator

$$a(t) = \begin{cases} \cos \pi t/2T & |t| < T \\ 0 & \text{otherwise} \end{cases} \qquad (8)$$

The resultant waveforms for $h_1(t)$ and $h_2(t)$ is shown in Figure 6.

The same set of filters can be used for SMSK/2 modulation and the resultant demodulated waveforms at various points of the receiver is shown in Figure 7.

SMSK/2 Performance in Additive White Gaussian Noise

The ideal performance for SMSK/2 using the filters defined by (6), (7) and (8) can be easily determined. Given two consecutive symbols defined by any one of the possibilities in the phase tree, the probability of error in detecting θ_k is given by

$$P_\alpha = \frac{1}{2} \text{erfc}\left[\sqrt{\frac{E_b}{N_0}} \frac{1}{T} \int_{-T}^{T} \cos(\alpha)a(-t)dt \right] \qquad (9)$$

where α represents the particular phase trajectory under consideration. This must be averaged over all possible phase trajectories to obtain $\overline{P}_\alpha$. Finally, since the final bit detection must be done differentially, the probability of error is given by $P_E = 2\overline{P}_\alpha(1-\overline{P}_\alpha)$.

However, this penalty can be avoided if the modulator NRZ sequence is first encoded such that the encoded output is one if $d_k \neq d_{k-1}$ and 0 if $d_k = d_{k-1}$. If this is the case, then the last step in Figure 5 can be avoided.

Figure 8 shows the simulated performance of SMSK/2 under an idealized additive white Gaussian noise assumption. Notice the degradation at 10^{-4} is about 0.4 dB. The corresponding degradation for

35.
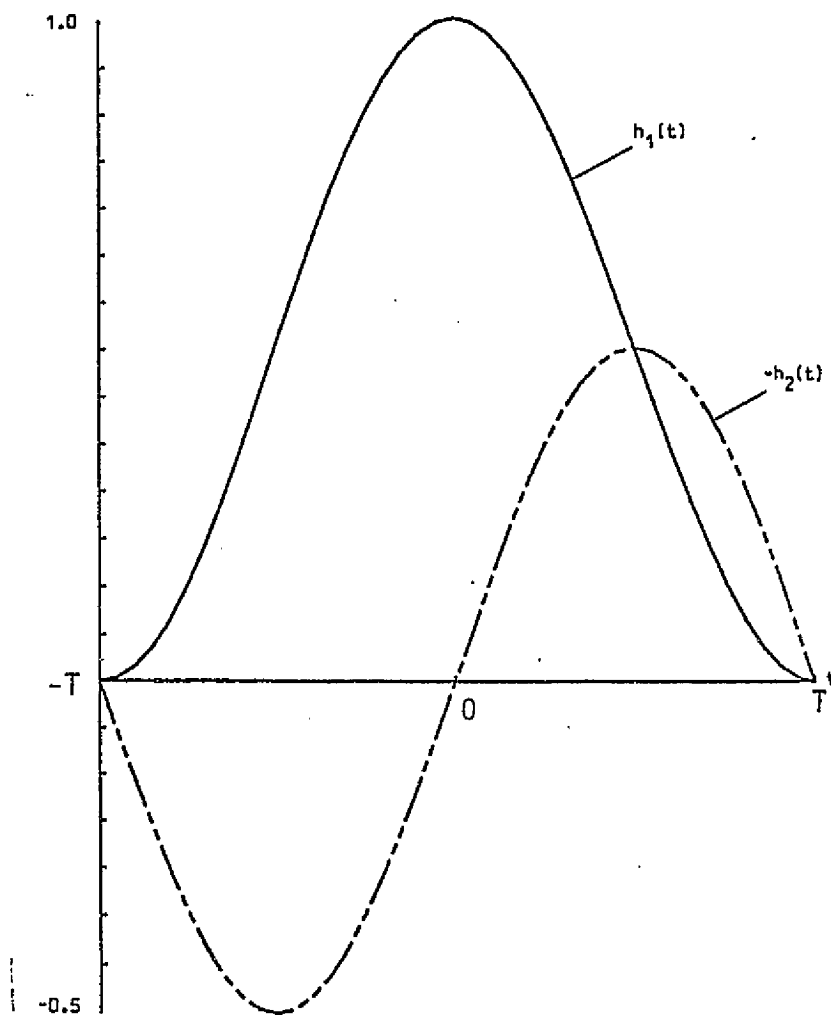
Figure 6.   Impulse responses of the filters to a serial
            MSK receiver.
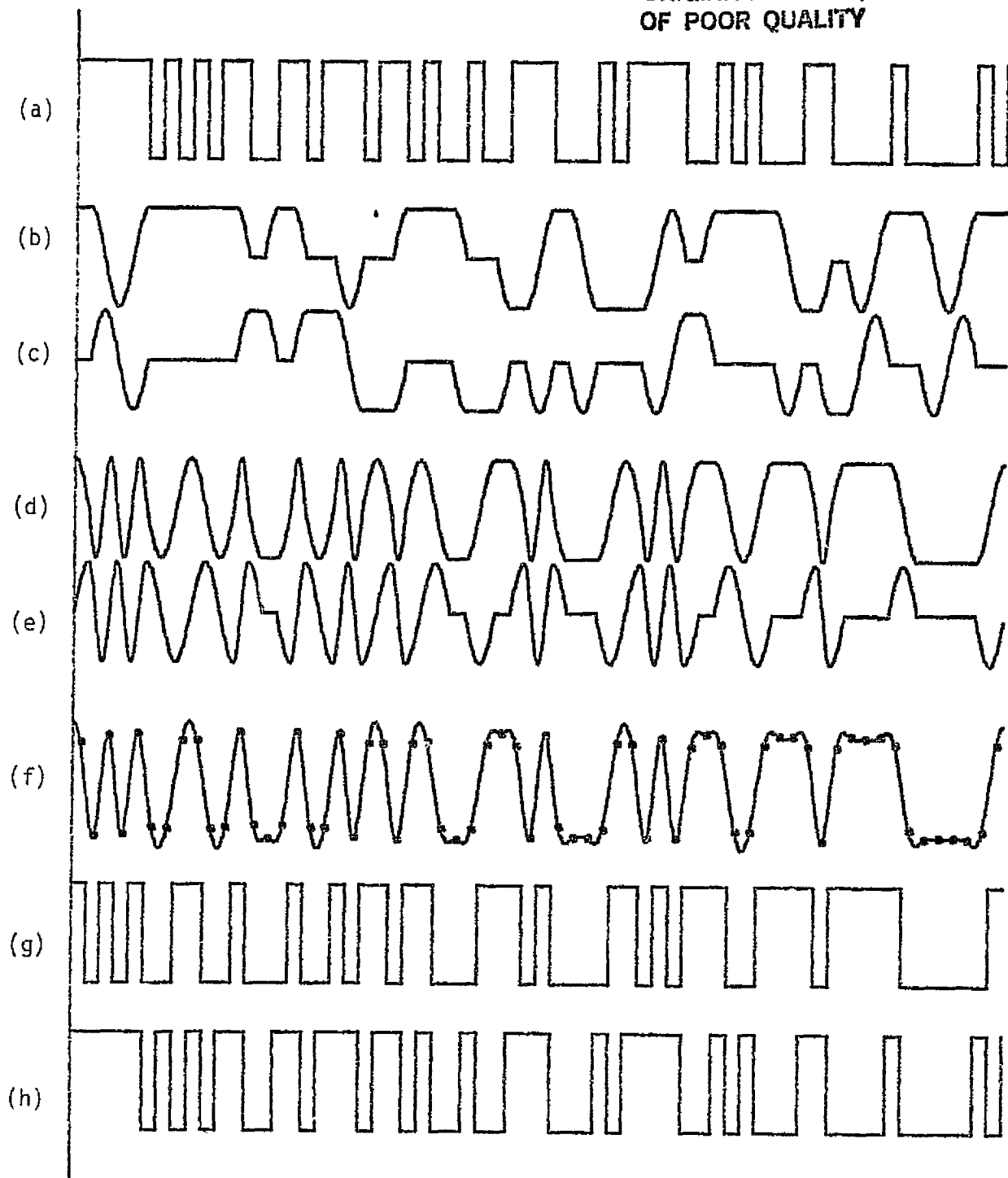
Figure 7.   Various wave forms at the SMSK/2 demodulator.   (a) Data sequence.
(b) & (c) I & Q components of modulator output (d) & (e) I & Q
components after demodulation (f) matched-filter output (g) Sampled
decisions α_k (h) reconstructed data $\hat{d}_k$.

Figure 8.   SMSK/2 Performance in Additive white Gaussian Noise
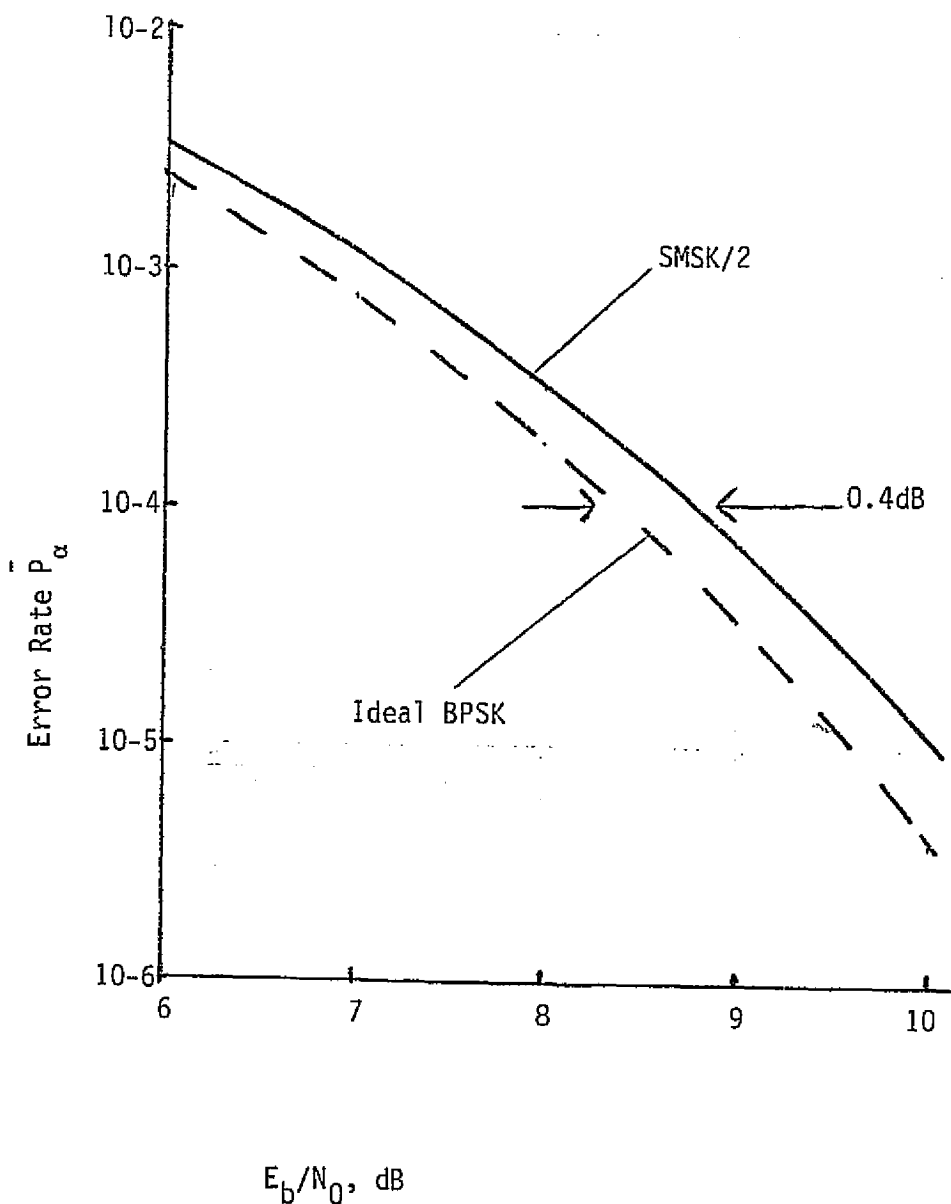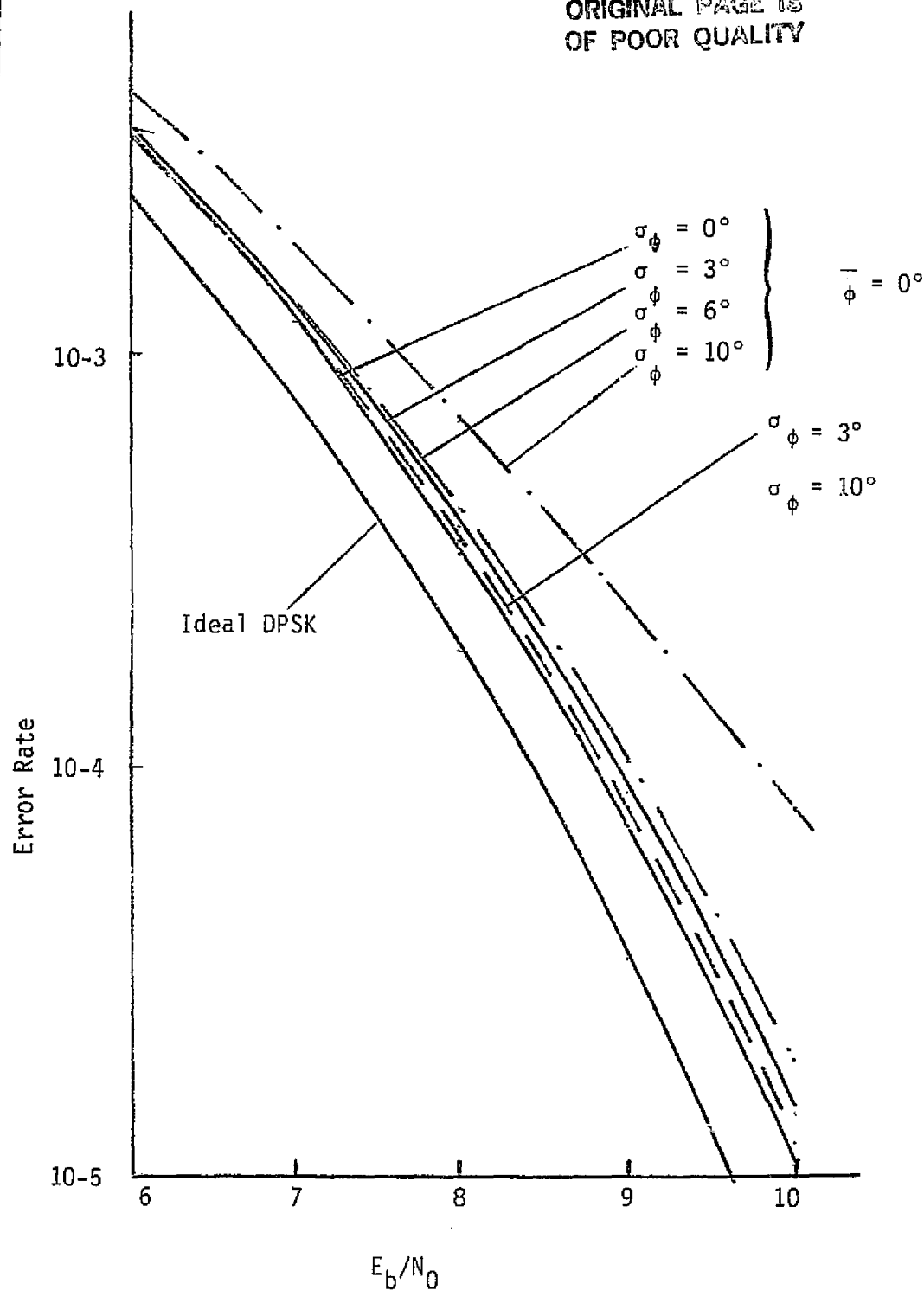
Figure 9.   SMSK/2 Sensitivity to Static Carrier Phase offset and
            Phase Jitter

8PSK is about 3.6 dB. Figure 9 shows the sensitivity of SMSK/2 to mean
carrier phase offset $\bar{\phi}$ and rms phase jitter. The performance is less
sensitive than 8PSK.

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REFERENCES

[1] T. Aulin and C. E. Sundberg, "Continuous Phase Modulation (CPM)-- Part I: Full Response Signaling," <u>IEEE Trans. Comm.</u>, Vol. COM-29, pp. 196-209, March 1981.

[2] T. Aulin, N. Rydbeck, and C. E. Sundberg, "Continuous Phase Modulation (CPM)--Part II: Partial Response Signaling," <u>IEEE Trans. Comm.</u>, Vol. COM-29, pp. 210-225, March 1981.

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APPENDIX II

MOTOROLA SMSK/2 MODEM

MOTOROLA INC.

Government Electronics Division

PERFORMANCE COMPARISON OF 8PSK AND SMSK/2

IN A SEVERELY BAND LIMITED CHANNEL

17 November 1983

Prepared by:

Carl R. Ryan, Manager
Communications Research
 Facility
(602)892-2100

Performance Comparison of 8PSK and SMSK/2

in a Severely Band Limited Channel

ABSTRACT

8PSK and SMSK/2 modem designs were compared and found to
have similar bit error rate performance in a system with no
hardware constraints considered. The SMSK/2 modem is
more tolerant to realistic hardware constraints, such as,
AM/PM conversion and demodulator phase error.

A rate 7/8 threshold codec used in the system provides
approximately 3dB improvement in the SMSK/2 system resulting
in a ideal Eb/No requirement of 12.5dB for 10^{-7} BER.
Realistic hardware constraints results in approximately 2dB
degradation from the 12.5dB performance.

Performance Comparison of 8PSK and SMSK/2

in a Severely Band Limited Channel

1.0   INTRODUCTION

This technical memo provides an analysis through
computer simulation of two possible modulation candidates for
a satellite communication channel.   The candidates are the
conventional 8PSK modulation format and the SMSK/2 modulation
format developed by Motorola.   The SMSK/2 power spectral
density is identical to that of duobinary linear phase
modulation with a modulation index of .5.   The SMSK/2 modem
has been configured to simplify hardware design and minimize
performance impairments due to hardware imperfections. The
Appendix is a detailed description of the modulation.

The computer simulation results indicate that the SMSK/2
format will require 1 to 3 dB less power than 8PSK when
operated in identical channels with an RF bandwidth of
approximately 1/2 the data rate.

The analysis technique used here is computer simulation
in which both linear and non-linear parameters are included
in the model.   The use of threshold coding is included in the
performance assessment and it is shown that a rate 7/8
threshold codec will provide 2 to 3 dB Eb/No improvement when
operating at a BER of 10^{-7}.

2.0   CHANNEL MODEL

The channel model chosen for the performance evaluation

is illustrated in Figure 2.1. This model is a reasonalbe
approximation to the satellite repeater and ground station.
Table 2.1 gives the 3 dB RF bandwidth and filter type of each
filter. All filters are normalized to the operating symbol
rate. The power amplifier characteristics are illustrated in
Figure 2.2.
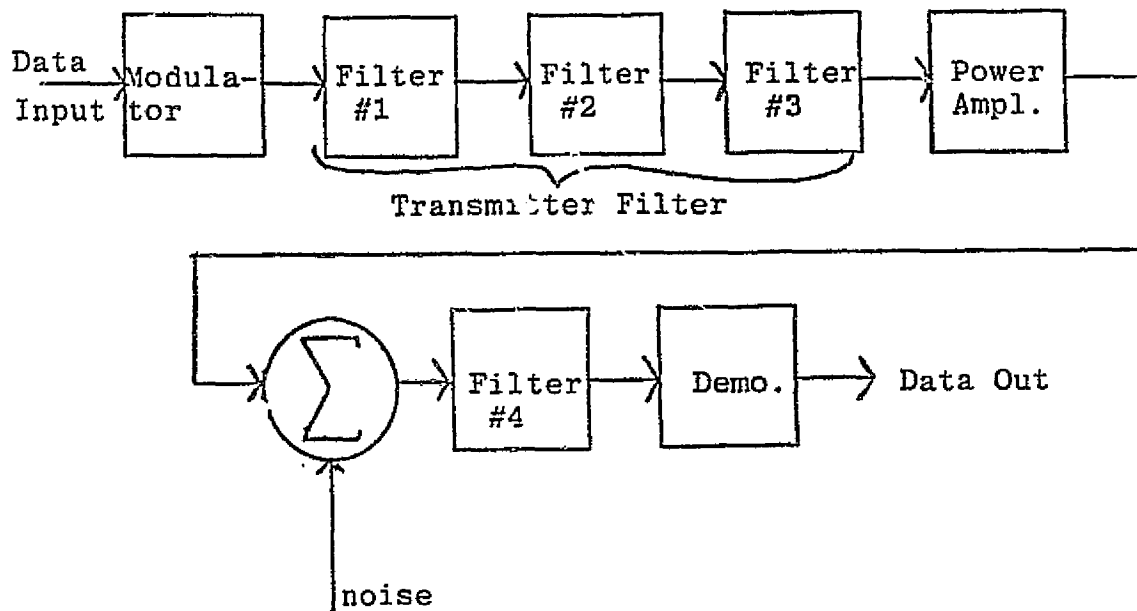
Figure 2.1   Channel Model
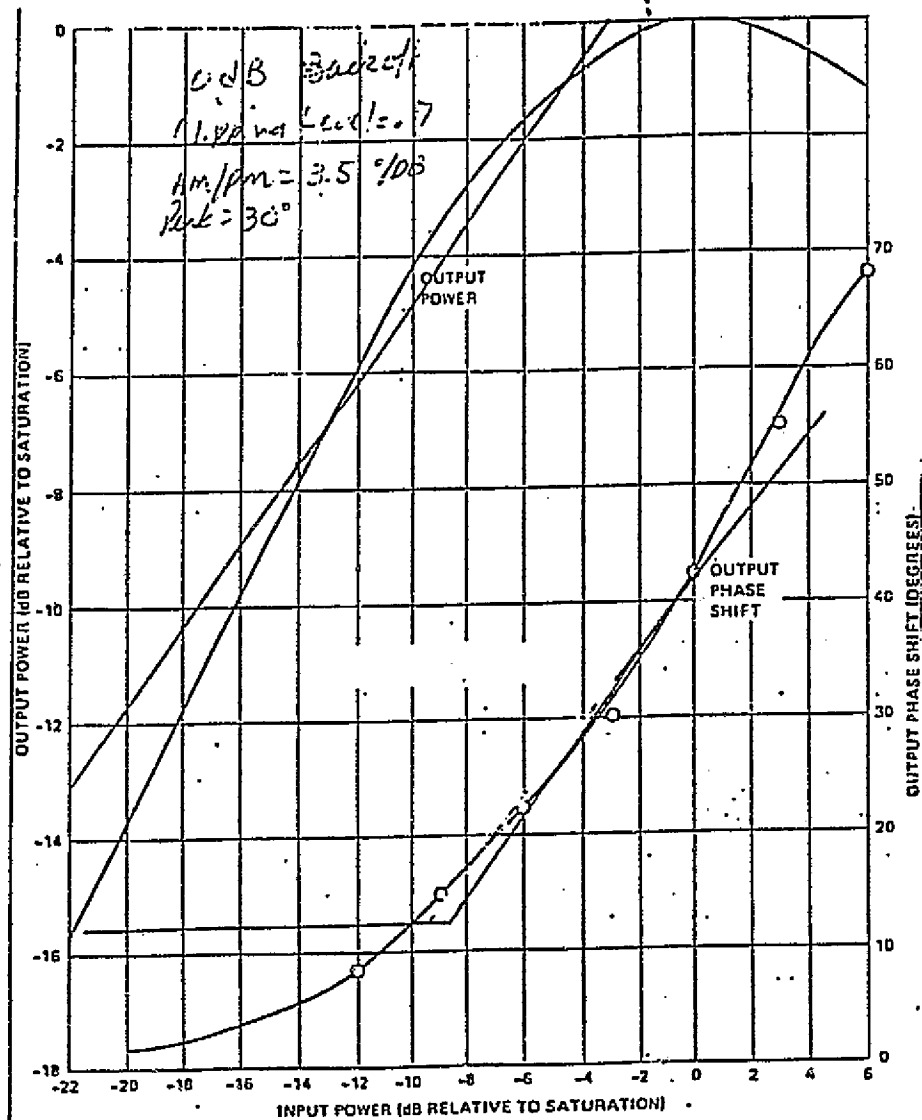
Figure 2.2   Model Non-Linear Amplifier Input-Output
Characteristics

Table 2.1   Filter Characteristics

Relative Symbol Rate	Filter #1 5 Pole Butterworth	Filter #2 5 Pole Butterworth	Filter #3 5 Pole Butterworth	Filter #4 5 Pole Butterworth	ChannelEfficiency (data rate divide by noise bandwid of transmitter filter)
.83	.59	.59	.51	.59	2.1
1.0	.49	.49	.45	.49	2.5
1.14	.43	.43	.39	.43	2.9

Note: The group delay of all filters has been equalized.

The frequency response and the impulse response of the 1.0 symbol filter is provided in Figures 2.3 and 2,4. The filter, F4, is used as the only receiver filter and therefore sets the demodulation noise bandwidth.

3.0   TRANSMITTER OUTPUT CONDITIONS

Three different drive levels were used for the power amplifier corresponding to 0 dB , 3 dB and 6 dB back off. Table 3.1 provides the computer model parameters used in the simulation.

Table 3.2   Non-Linear Model Parameters

Input Backoff	Effective Clipping Level	AM/PM Conversion in degrees/dB	Peak Phase Change
0dB	.7	3.5	30
3dB	1.0	2.8	25
6dB	1.4	2.5	15

The transmitter envelope amplitude for SMSK/2 is illustrated in Figures 3.1 and 3.2 for the 1.0 and 1.14 symbol rates.

4.0   RECEIVER OUTPUT

The receiver output characteristics for SMSK/2 are presented in Figures 4.1 through 4.6.   The data presented
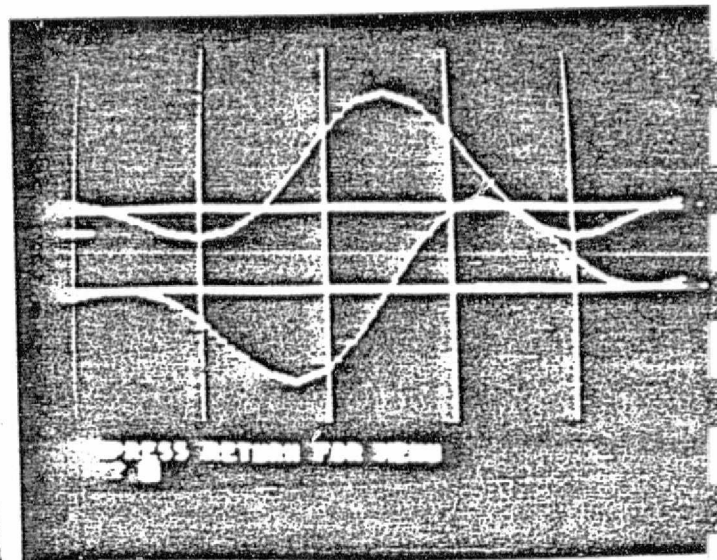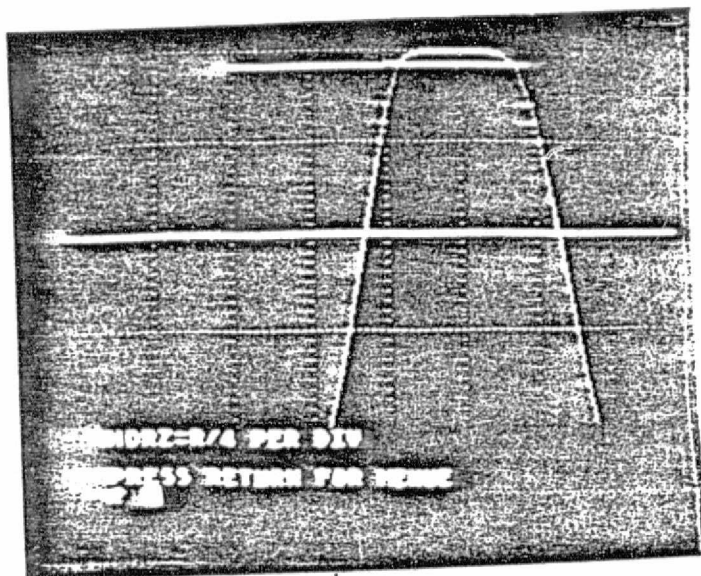
(a)   (b)

Figure 2.3   1.0 Symbol Rate F1, F2, and F3 Cascade
        (a) 20dB/div Vertical R/4 per division Horizontal
        (b) $\frac{1}{R}$ per division horizontal
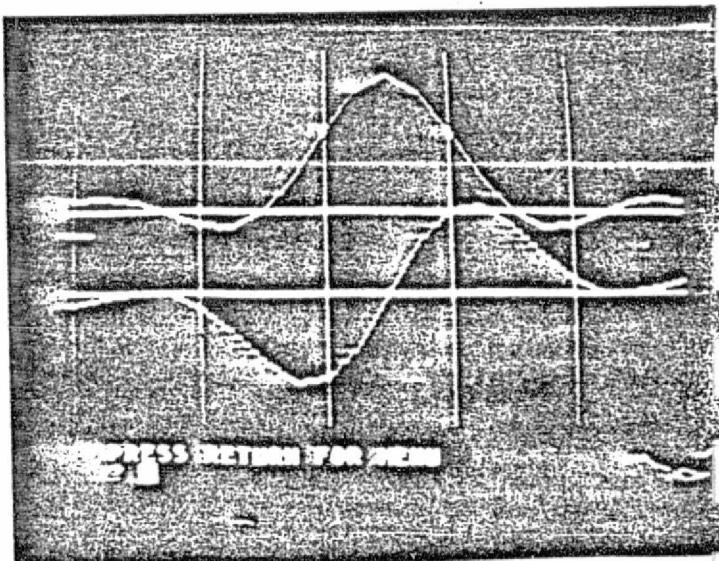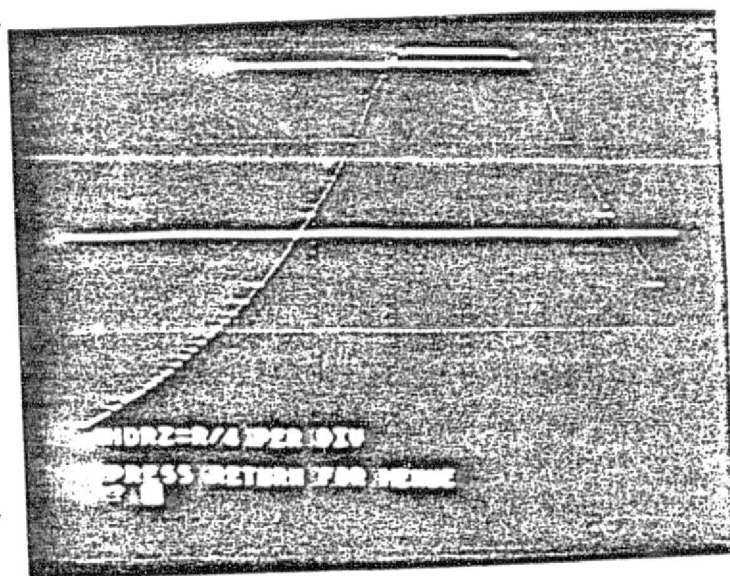
Figure 2.4   1.0 Symbol Rate F4.   Same scale as Figure 2.3
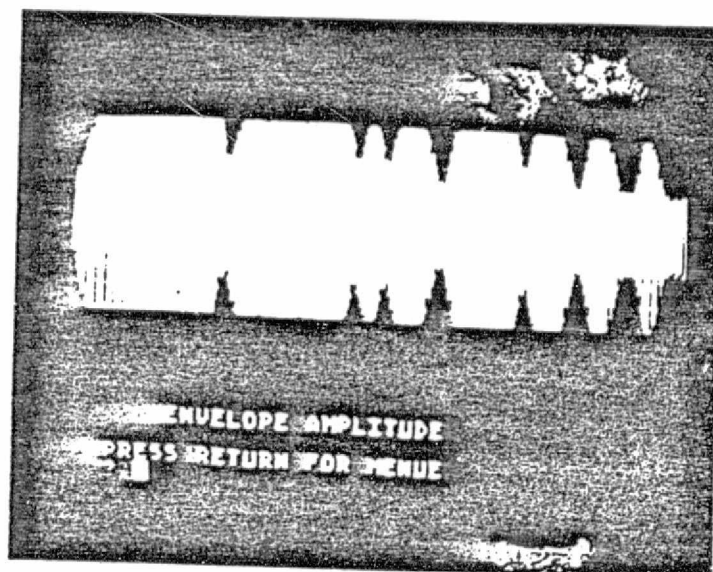
Figure 3.1   Xmt out
             3dB Backoff
             1.0 Symbol Rate
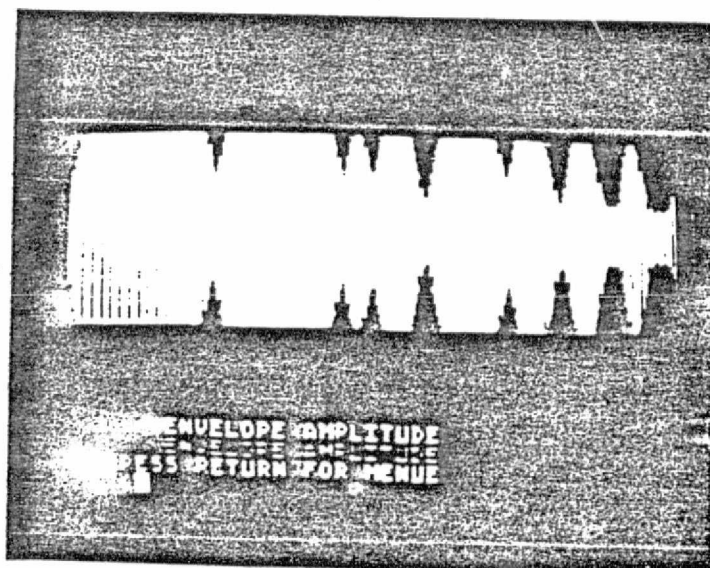
Figure 3.2   Xmt Out
             3dB Backoff
             1.14 Symbol Rate

Figure 4.1

0dB Backoff   .83 Symbol Rate
(Highside Reference)

Figure 4.1a   Receiver
              Envelope Amplitude
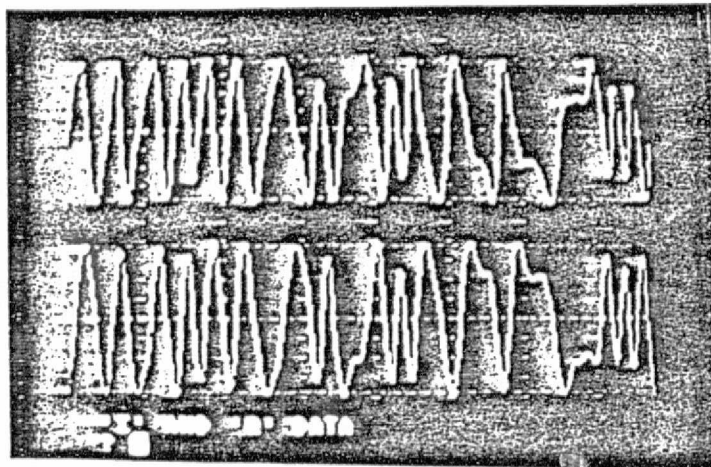
Figure 4.1b   I&Q Waveforms
              Phase = 22°
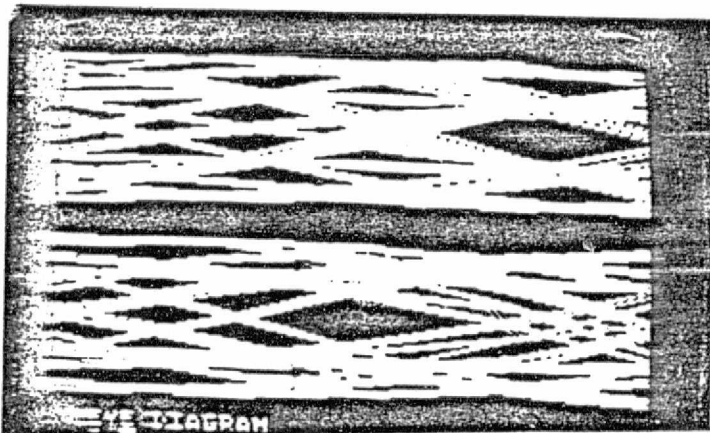
Figure 4.1c   I&Q Eye Patterns
              Phase = 22°
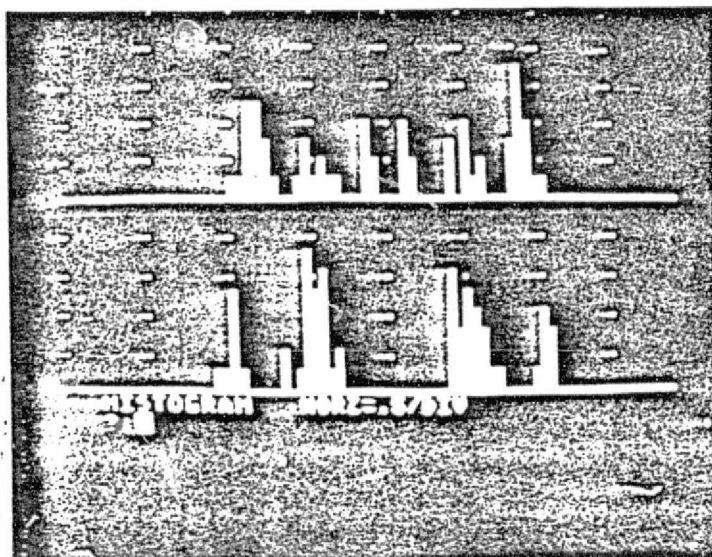
Figure 4.1d   Histogram for
              Phase = 22°
              Sample Time = .8

Figure 4.2

OdB Backoff   .83 Symbol Rate
(Lowside Reference)
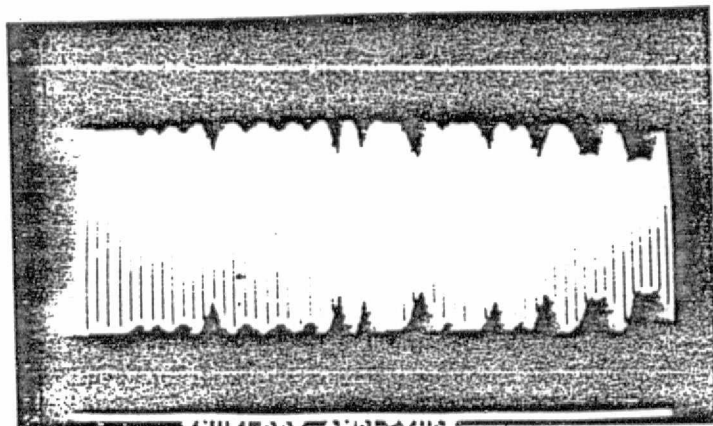
Figure 4.2a

Receiver Envelope
Amplitude

Figure 4.2b

I&Q Waveforms
Phase = 6°
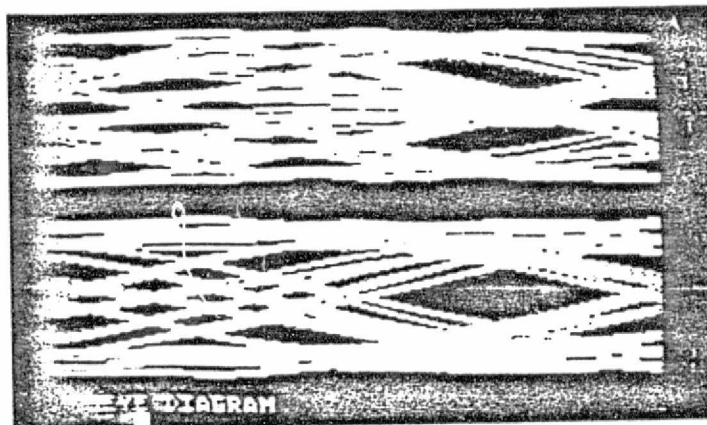
Figure 4.2c   I&Q Eye Patterns
Phase = 6°
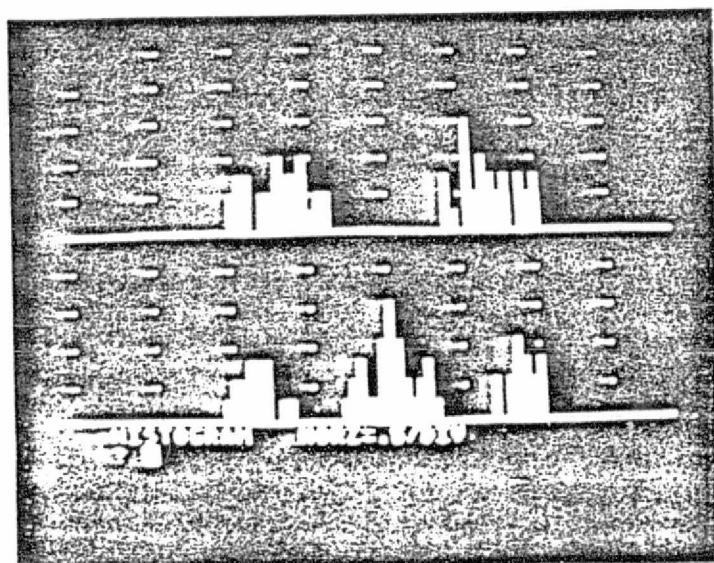
Figure 4.2d   Histograms for
Phase = 6°
Sample Time = .7

Figure 4.3

3dB Backoff
1.0 Symbol Rate
(Highside Reference)

Figure 4.3a Receiver Envelope
Amplitude
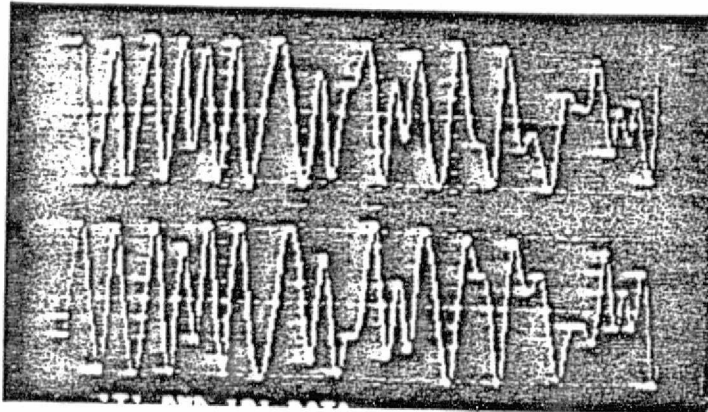
Figure 4.3b I&Q Waveforms
Phase = 34°
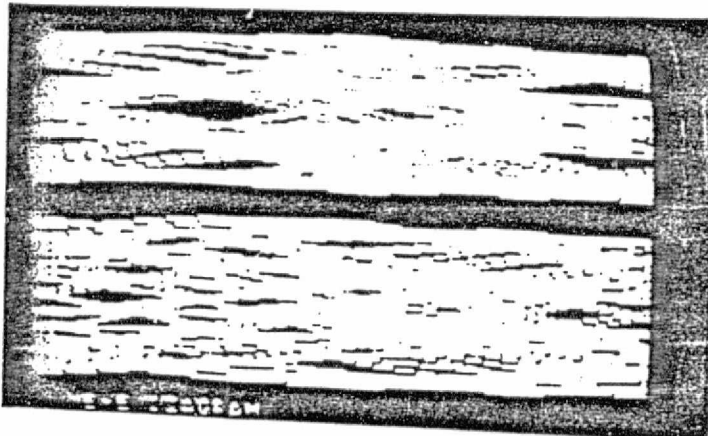
Figure 4.3c Eye Patterns
Phase = 34°
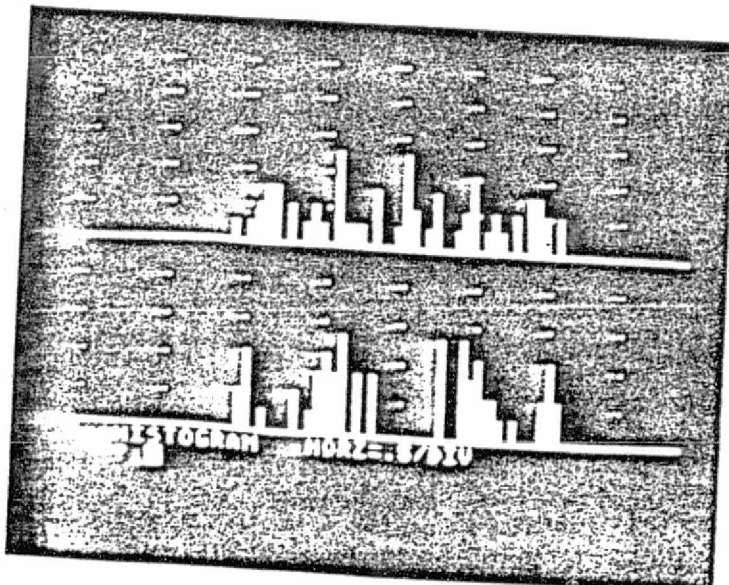
Figure 4.3d Histogram for
Phase = 34°
Sample Time = 1.25
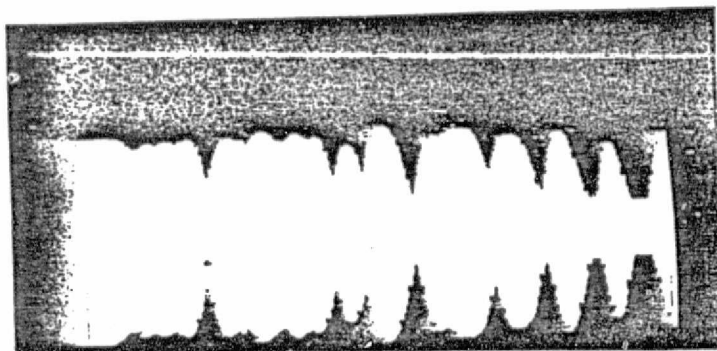
Figure 4.4

3dB Backoff
1.0 Symbol Rate
(Low Side Reference)

Figure 4.4a Receiver Envelope
Amplitude

Figure 4.4b I&Q Waveforms
Phase = 22°
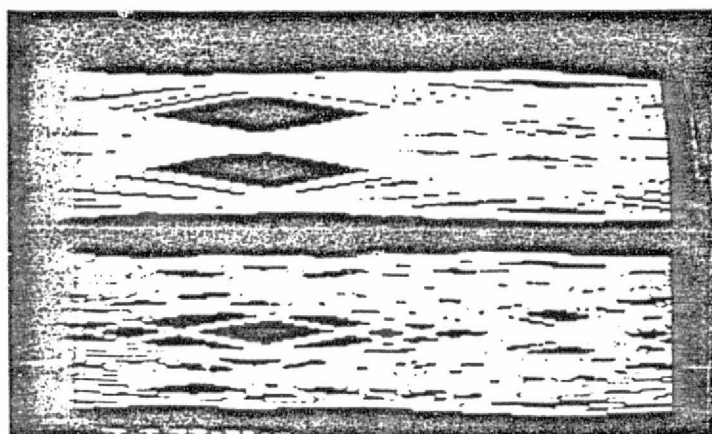
Figure 4.4c Eye Patterns
Phase = 22°
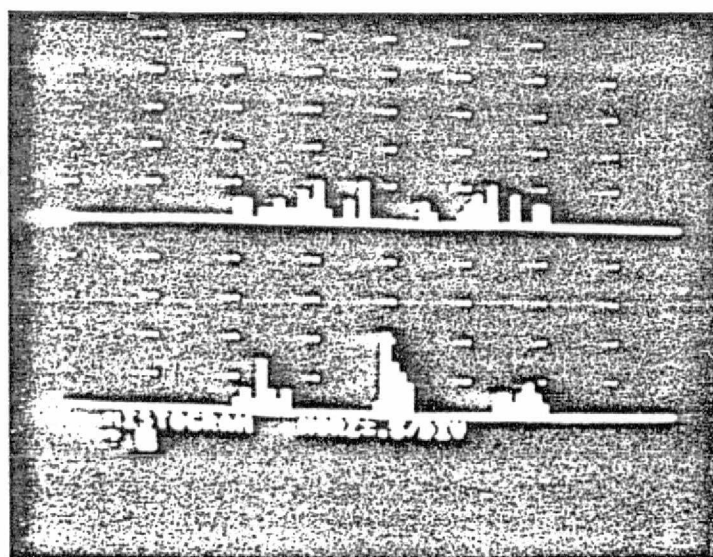
Figure 4.4d Histogram
Phase = 22°
Sample Time = 1.3
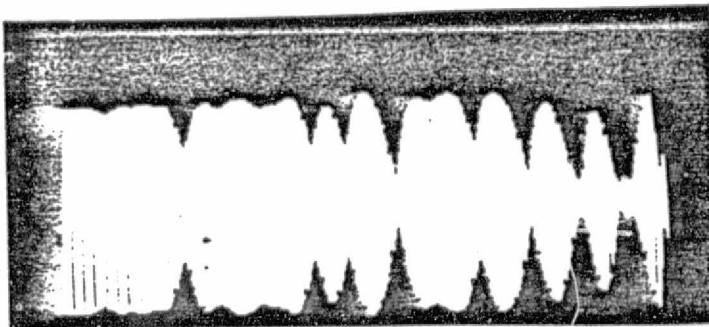
Figure 4.5

3dB Backoff
1.14 Symbol Rate
(High Side Reference)

Figure 4.5a Reveiver Envelope
            Amplitude

Figure 4.5b I&Q Waveforms
            Phase = 32°
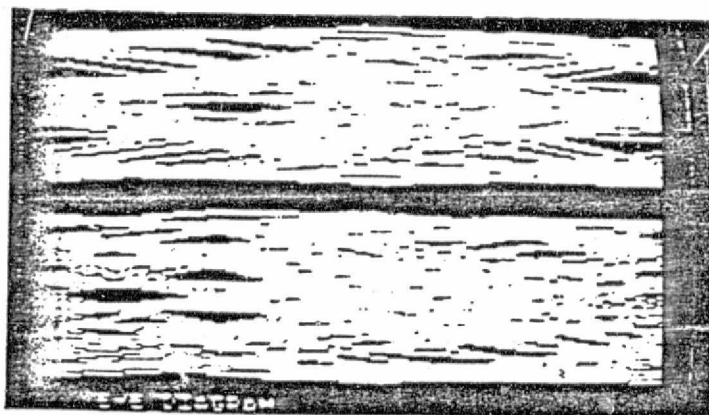
Figure 4.5c Eye Patterns
            Phase = 32°
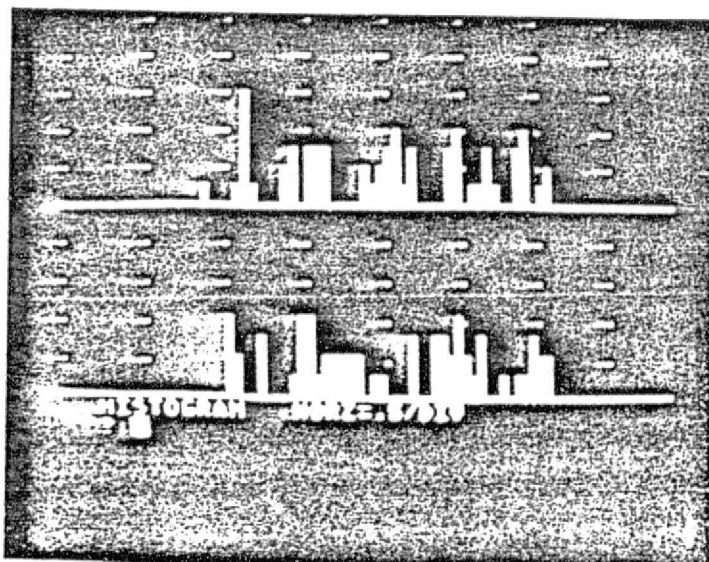
Figure 4.5d Histogram
            Phase = 32°
            Sample Time = 1.25

Figure 4.6

3dB Backoff
1.14 Symbol Rate
(Low Side Reference)

Figure 4.6a   Receiver Envelope
              Amplitude

Figure 4.6b   I&Q Waveforms
              Phase = 4°
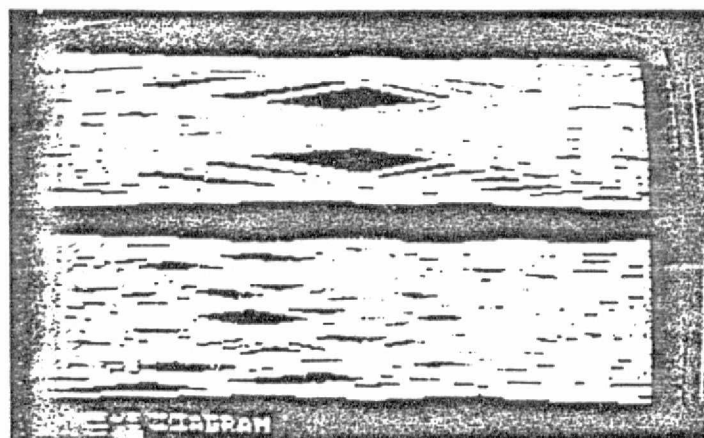
Figure 4.6c   Eye Patterns
              Phase = 4°
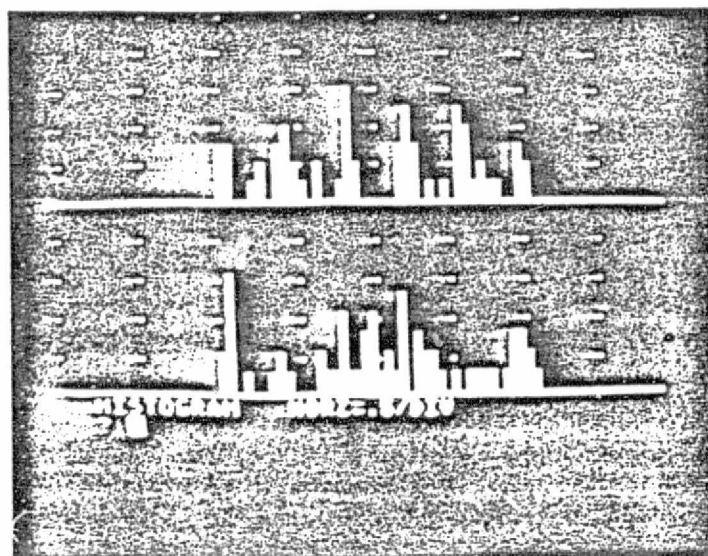
Figure 4.6d   Histogram
              Phase = 4°
              Sample Time = 1.3

includes the received envelope amplitude, the I and Q data waveforms, EYE patterns, and the histogram. The I and Q waveforms and the EYE patterns are displayed at the optimum phase. The histogram is the display of the sample points at the optimum sample time and the optimum phase test conditions for each example is included in the figures.

Different performance was obtained depending on whether the phase reference was used on the high side or the low side. Results of these two conditions are illustrated.

5.0   BIT ERROR RATE PERFORMANCE

The Bit Error Rate performance of the SMSK/2 modem was obtained from the computer simulation for various operating conditions. The following conditions were used.

1.   Data: 110 Bits of data from a 7 stage maximum length PN generator.

2.   All power reference is based on Peak power out of the power amplifier.

3.   The optimum carrier phase and symbol timing performance was obtained and used as the timing reference point.

4.   The rate 7/8 code (DITEC) was used for the coded performance measurements. The performance of this code is presented in Figure 5.1.

5.1   SYMBOL ERROR RATE

The Symbol Error Rate for the SMSK/2 modem for various operating conditions is presented in Figure 5.2 for the 0 dB backoff condition and in Figure 5.3 for the 3 dB backoff
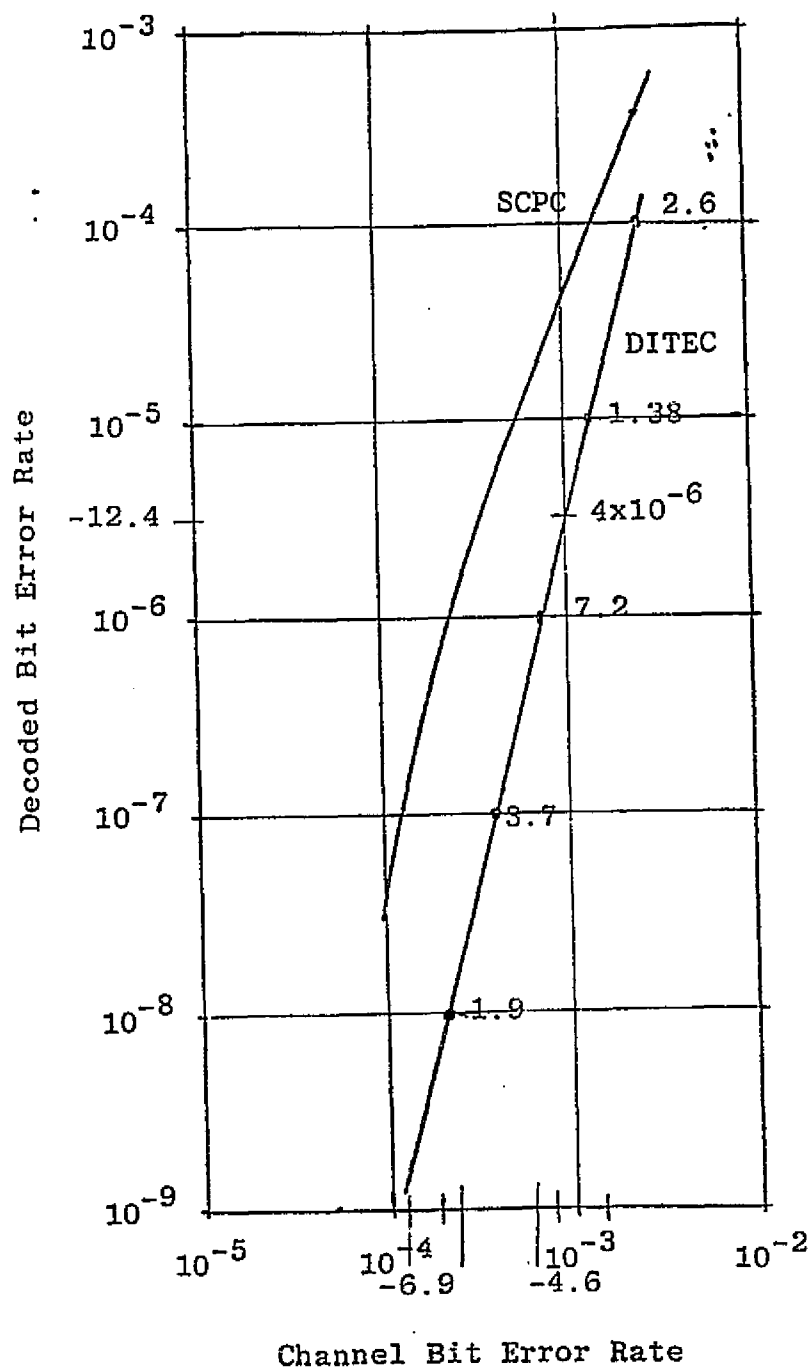
Figure 5.1 Error Rate of Rate 7/8 Codes
with Threshold Decoding

C-2

1. .83R Low Side Ref.   4. 1.0R High Side Ref.
2. .83R High Side Ref.   5. 1.14R Low Side Ref.
3. 1.0R Low Side Ref.   6. 1.14R High Side Ref.
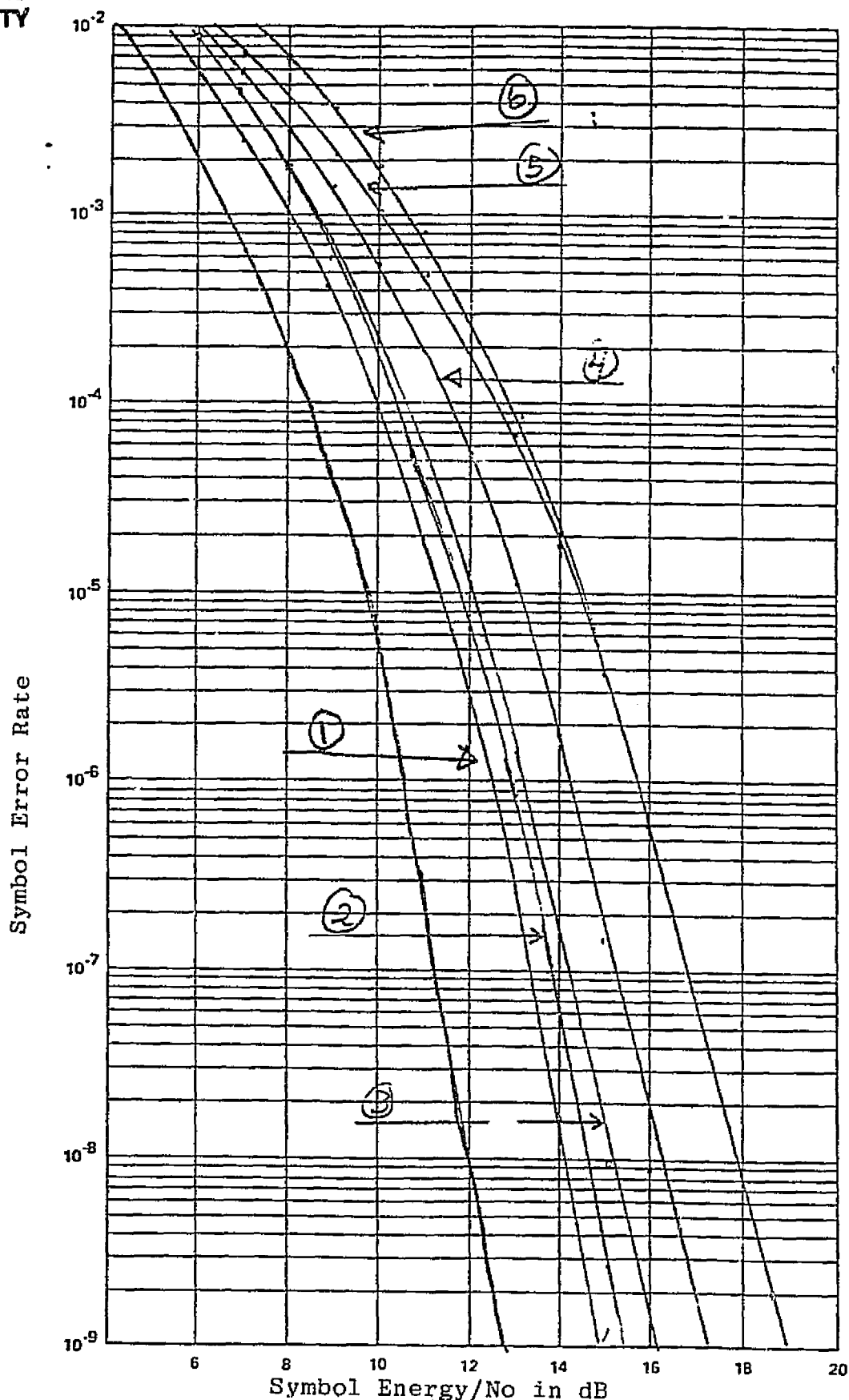
Figure 5.2   SMSK/2 Bit Error Rate vs Eb/No for 0dB
Backoff TWTA Operation.

3. 1.0R Low Side Reference   6. 1.14R High Side Reference
4. 1.0R High Side Reference
5. 1.14R Low Side Reference
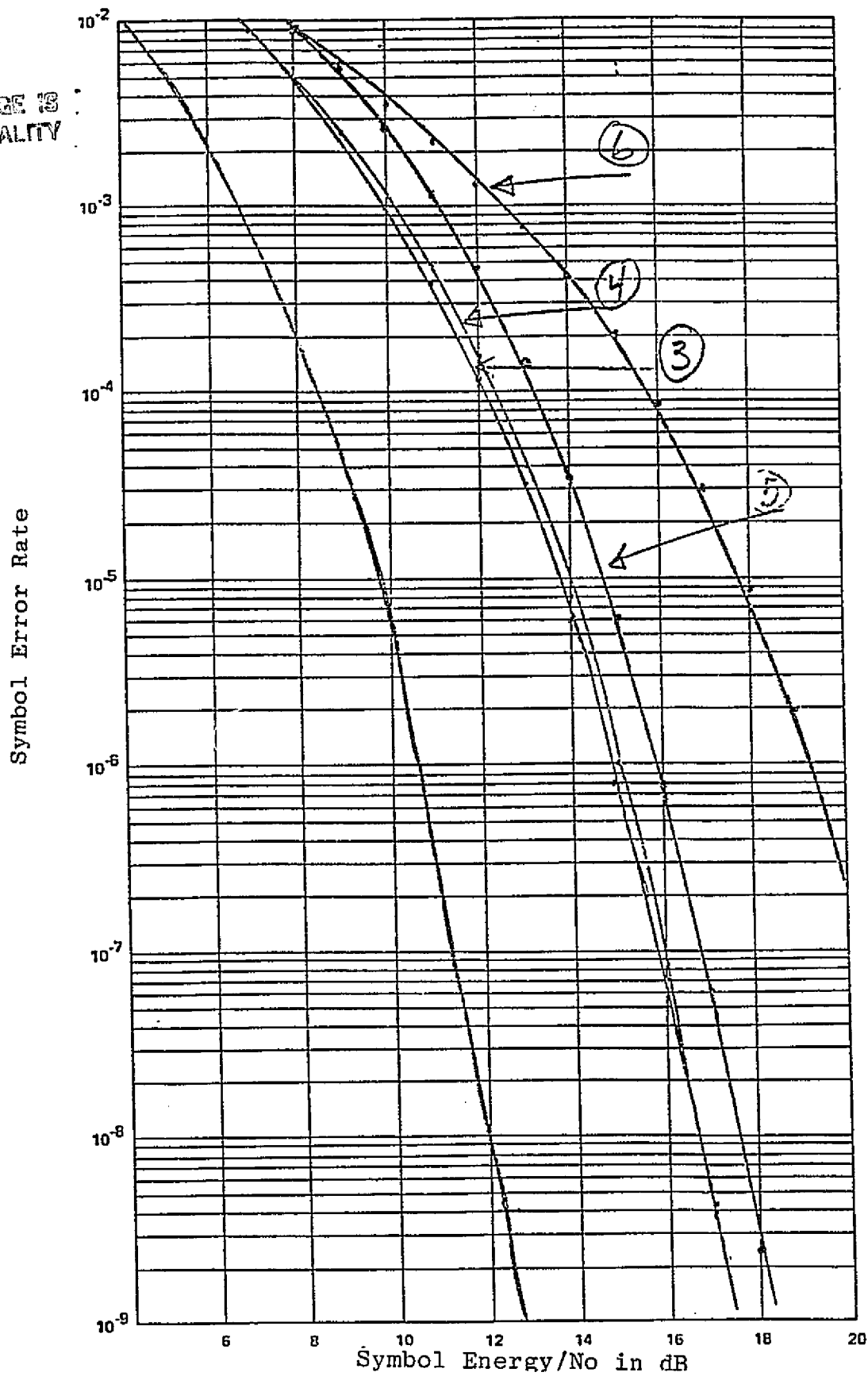
Figure 5.3   SMSK/2 Bit Error Rate Vs Eb/No for
3dB Backup

condition.

Note that in all cases the low side carrier phase reference performed as good or better than the high side carrier phase reference.

5.2   CODED VS UNCODED PERFORMANCE

The modem performance was evaluated on the basis of its coded vs uncoded BER vs Eb/NO. Figure 5.4 illustrates the results of this simulation. The test condition in this data is for the 3 dB TWTA backoff and optimum carrier and symbol timing.

Figure 5.5 illustrates the timing sensitivity of the uncoded system vs TWTA backoff based on obtaining a 10^{-7} BER. Figure 5.6 provides similar information for the coded condition. Figure 5.7 provides a comparison of the coded and uncoded timing sensitivity for different TWTA backoff conditions.

6.0   8PSK SYSTEM PERFORMANCE

The 8PSK system was evaluated for filters identical to that used in the SMSK/2 system and with identical coding conditions.

Figure 6.1 illustrates the coded vs uncoded BER performance of the system when the carrier phase and symbol timing are set to the optimum condition and for a 3 dB TWTA backoff condition. This result is almost identical to that obtained for the SMSK/2 as illustrated in figure 5.4.

Figure 6.2 illustrates the uncoded BER performance vs TWTA backoff for various timing errors. Figure 6.3
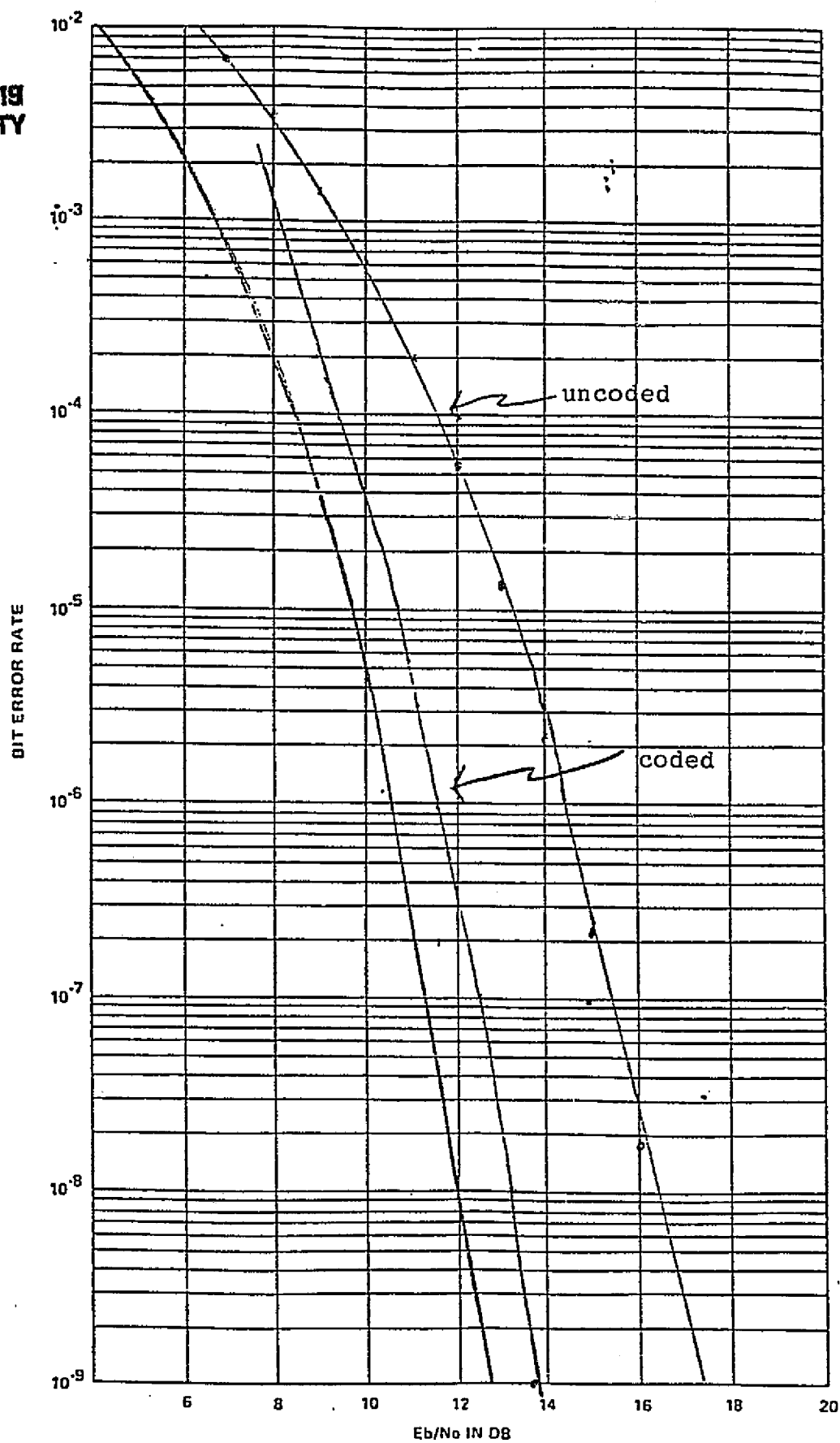
Figure 5.4   Coded vs Uncoded SMSK/2 for 3dB TWTA
             Backoff (Rate 7/8 Codec Used)
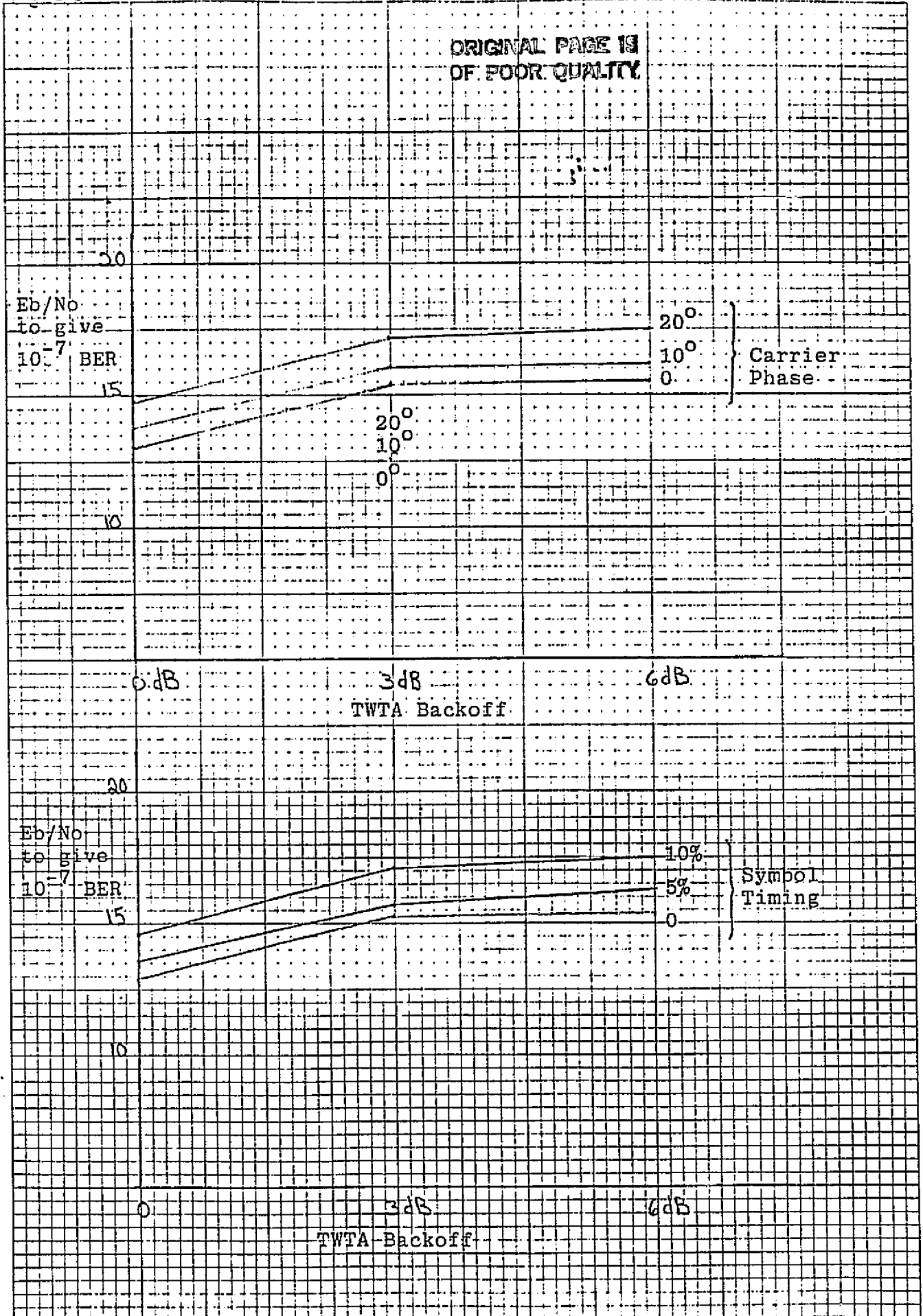
Figure 5.5   SMSK/2 Performance vs PA Backoff for Uncoded Systems
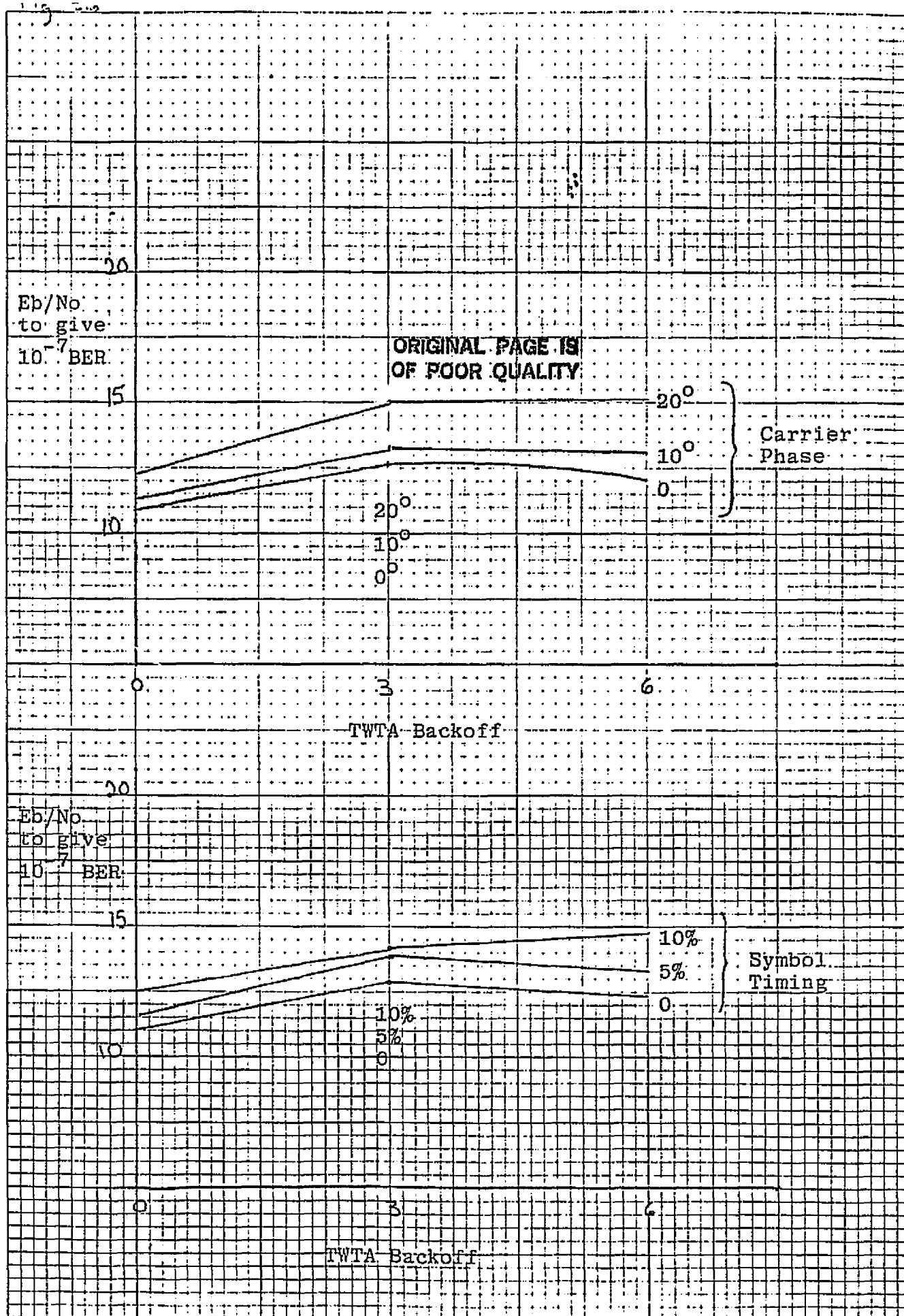
Figure 5.6   SMSK/2 Performance vs PA Backoff for Rate 7/8 <u>Coded</u> Systems
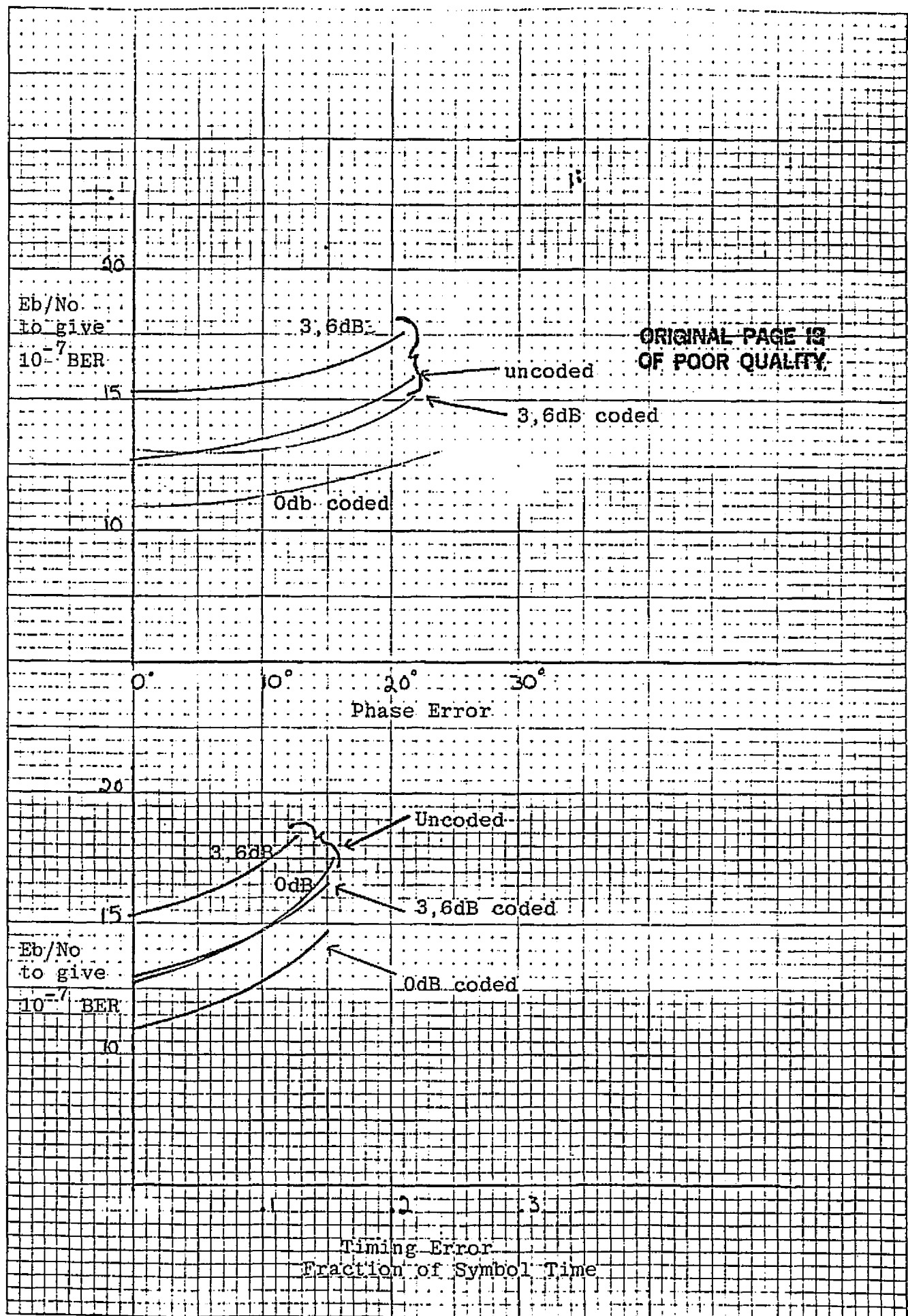
Figure 5.7   SMSK/2 Performance vs PA Backoff for <u>Uncoded</u> Systems
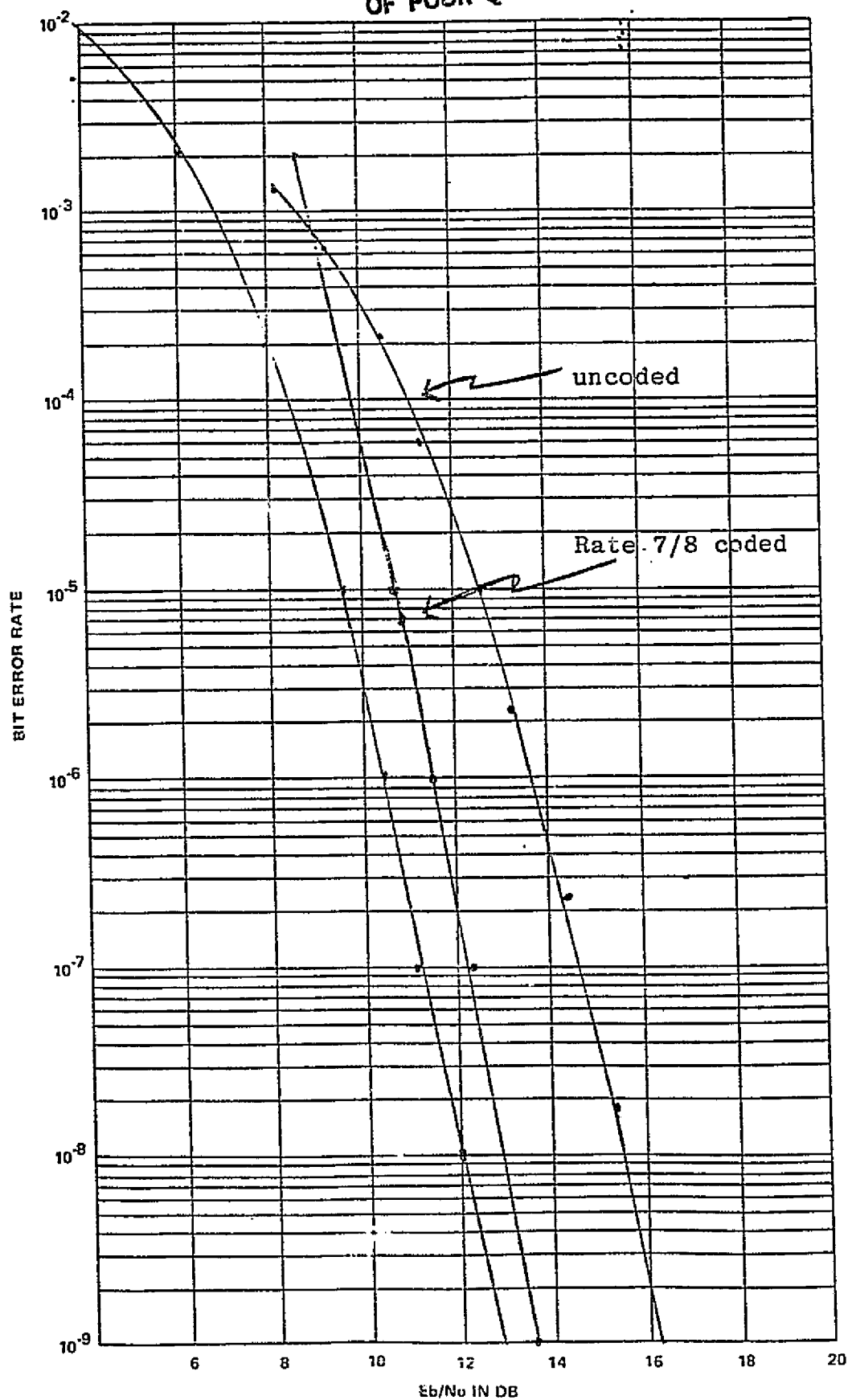
Figure 6.1   BER vs Eb/No for 3dB Backoff 8PSK - Optimum Timing
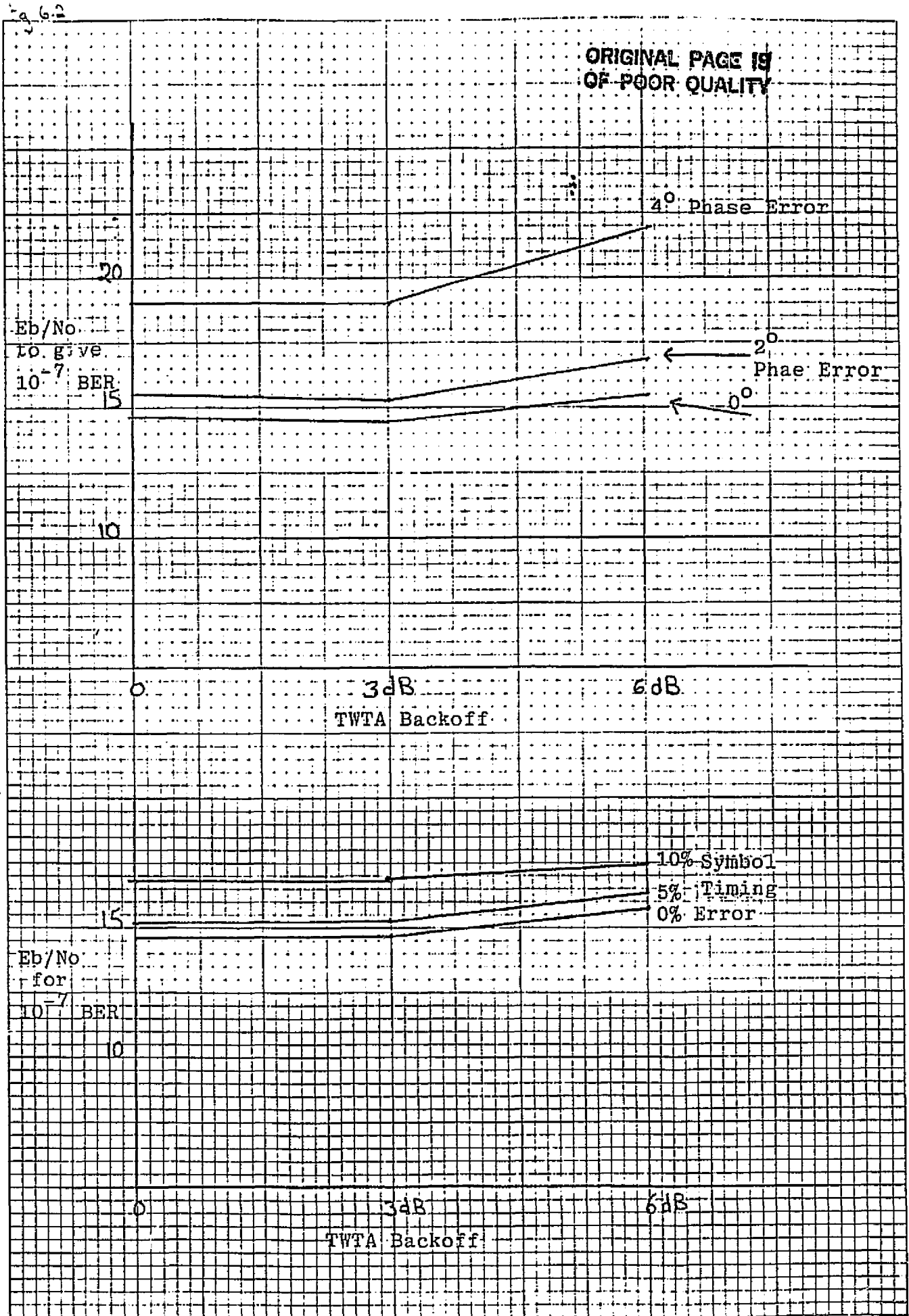
Figure 6.2   8PSK Performance vs PA Backoff for uncoded system
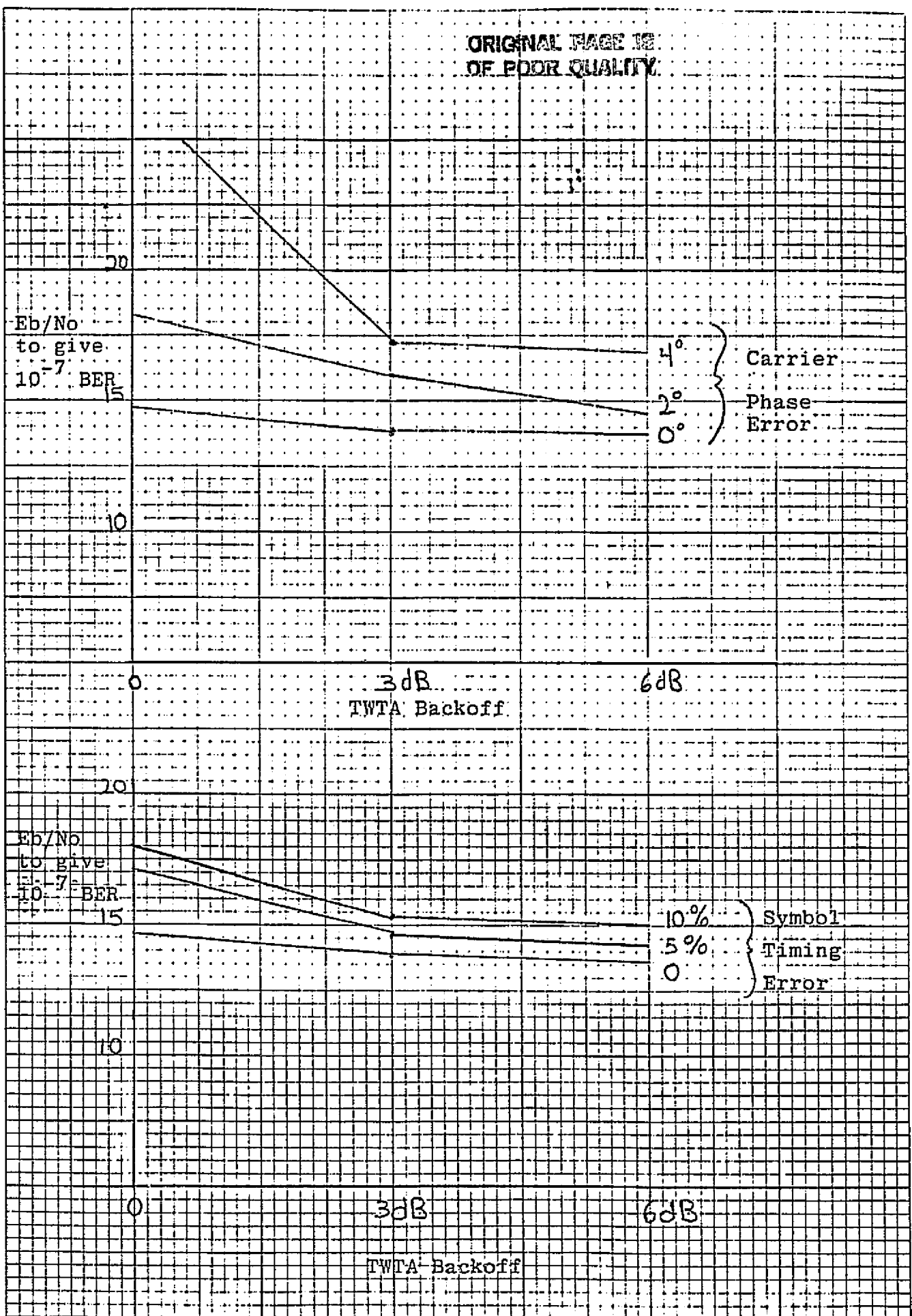
Figure 6.3   8PSK Performance vs PA Backoff for Rate 7/8 Coded System
for Different Phase and Timing Conditions
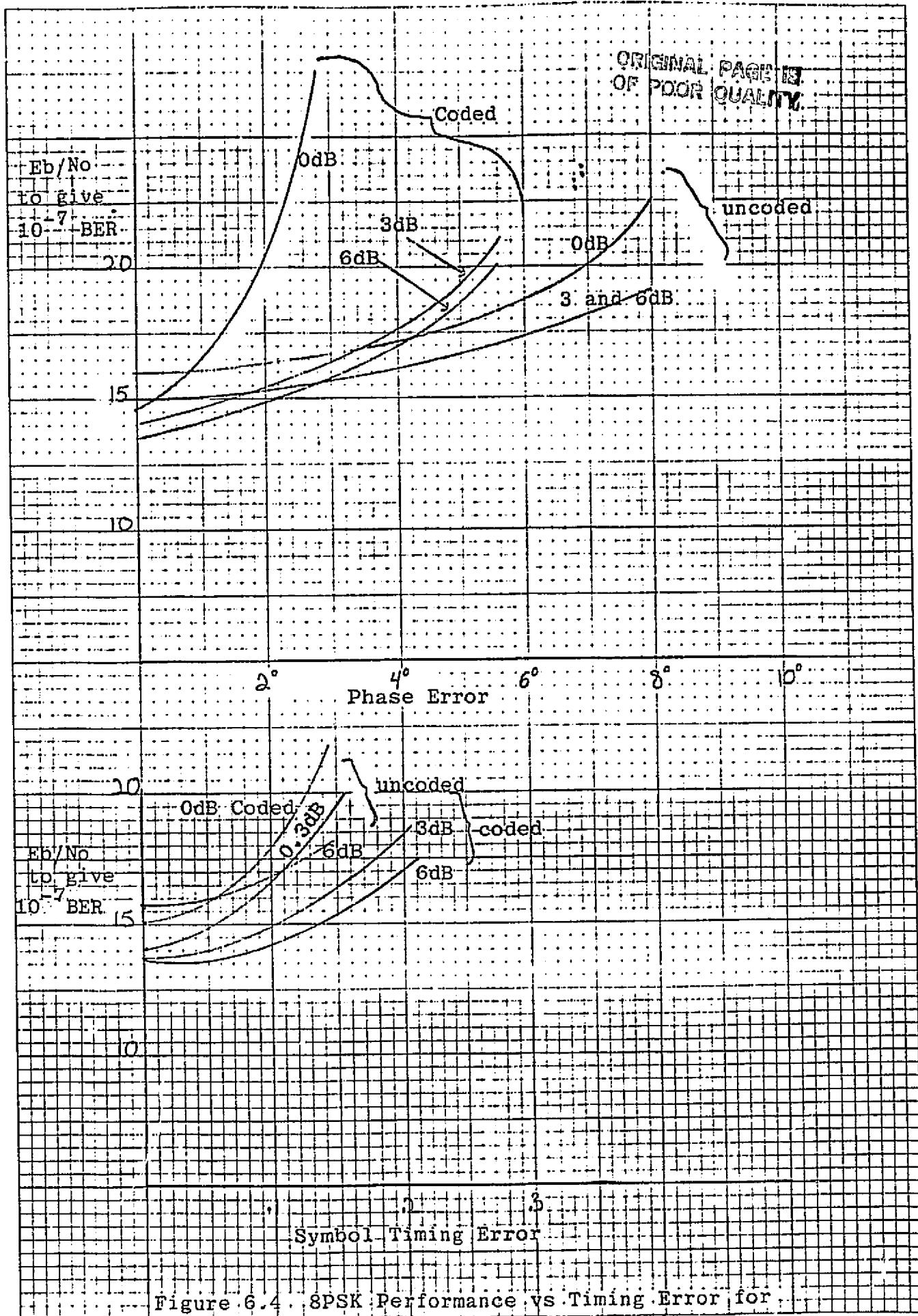
Figure 6.4. 8PSK Performance vs Timing Error for Various TWTA Backoff Conditions

illustrates the coded BER performance vs TWTA backoff for various timing errors. Figure 6.4 provides a comparison of the timing sensitivity for different TWTA backoff conditions.

7.0 SYSTEM PERFORMANCE ASSESSMENT

The system performance can be estimated based on realistic hardware considerations. Table 7.1 and 7.2 provide this comparison for the two schemes based on the coded and uncoded system. Table 7.1 represents an optimisitic estimate of the hardware performance. Table 7.2 represents a more realisitc estimate of the operational hardware. All estimates are based on 3 dB TWTA backoff.

A comparison of these two tables indicate that SMSK/2 is more tolerant to hardware distortions and that the 10^{-7} BER can be achieved with an Eb/No of less than 15 dB.

Table 7.1   Optimistic Hardware Performance

Parameter	Value	Degradation at 10^{-7} BER			
		uncoded		coded	
		8PSK	SMSK/2	8PSK	SMSK/2
Carrier Phase	2°	.5dB	0dB	1.5dB	0dB
Symbol Timing	2.5%	.4dB	.5dB	.2dB	.6dB
Decision Threshold	1%	.1dB	.1dB	.1dB	.1dB
Equalization Accuracy	–	.5dB	.5dB	.5dB	.5dB
Total Degradation		1.5dB	1.1dB	2.3dB	1.2dB
Ideal Eb/No Required for 10^{-7} BER		14.6dB	15.4dB	12.2dB	12.5dB
Resulting Eb/No		16.1db	16.5dB	14.5dB	13.7dB

Table 7.2 Realistic Hardware Performance

Parameter	Value	Degradation at 10^{-7} BER			
		uncoded		coded	
		8PSK	SMSK/2	8PSK	SMSK/2
Carrier Phase	4°	1.2dB	.1dB	4dB	.1dB
Symbol Timing	5%	.8dB	.7dB	.5dB	.8dB
Decision Threshold	2%	.2dB	.2dB	.2dB	.2dB
Equalizer Accuracy	–	.8dB	.8dB	.8dB	.8dB
Total Degradation		3.0dB	1.8dB	5.5dB	1.9dB
Ideal Eb/No Required for 10^{-7} BER		14.6dB	15.4dB	12.2dB	12.5dB
Resulting Eb/No		17.6dB	17.2dB	17.7dB	14.4dB

8.0 CONCLUSION

8PSK and SMSK/2 modem designs were compared and found to have similar bit error rate performance in an optimized system, however, the SMSK/2 is more tolerant to realistic hardware constraints and is therefore recommended for this satellite data modem application.

The rate 7/8 threshold codec provides approximately 3 dB improvement in BER performance over the uncoded system.

2 Bit/Hz Serial MSK/2 Modem

INTRODUCTION

This memo provides some details of the design of a 2
Bit/Hz Serial MSK Modem. The design has been configured to
allow for easy hardware implementation, have a constant
envelope amplitude, and require approximately 1.0dB more
Eb/No than a conventional MSK modem.

MODULATION FORMAT

The modulation format chosen for this design has an
excess phase trellis as illustrated in Figure 1. This is
basically a duobinary linear phase m=1/2 modulation format.
The Comparative Power Spectral densities for this modulation
format is illustrated in Figure 2. These figures illustrate
that the basic design chosen provides the 2 Bit/Hz bandwidth
efficiency. The sensitivity to carrier tracking errors is
similar to the SMSK modulation format.

SMSK/2 MODULATION

The SMSK/2 is a derivation of the SMSK modulation
format. The bandwidth efficiency is obtained by using three
phase states instead of two as in the SMSK format. This
through state format extends the remergence time from 2 to 3
bits, thus allowing for potential improvement in power
efficiency.
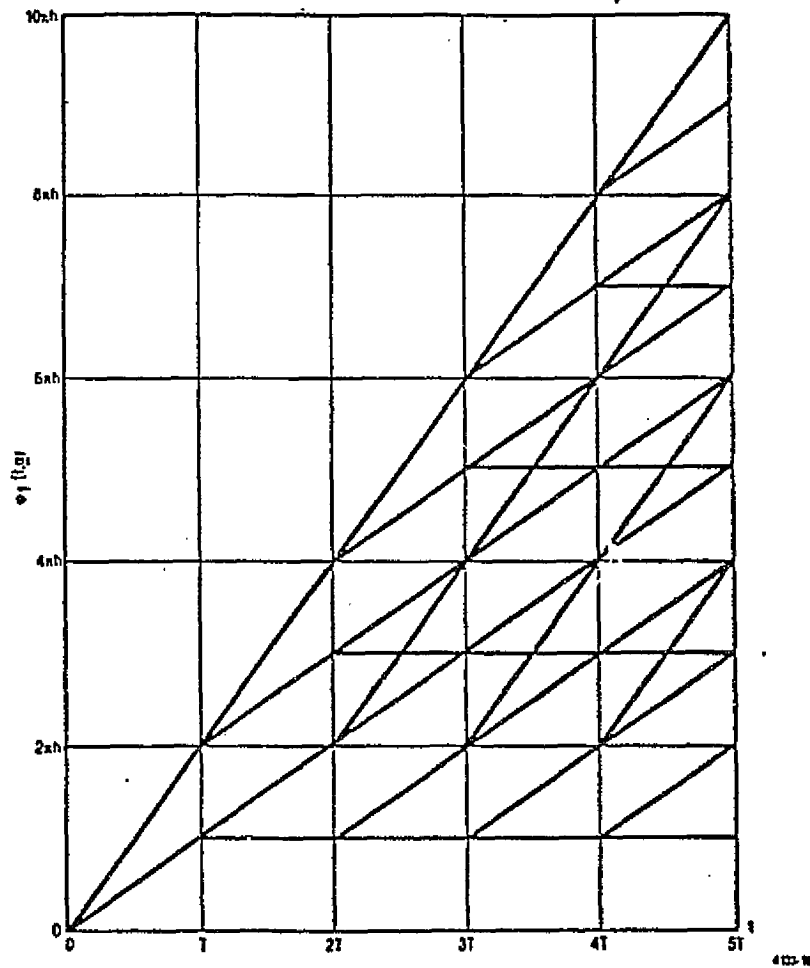
Figure 1   Phase Tree for a Serial Receiver
            for 2RFC

Figure 2   Comparisons of SMSK and SMSK/2 Waveforms
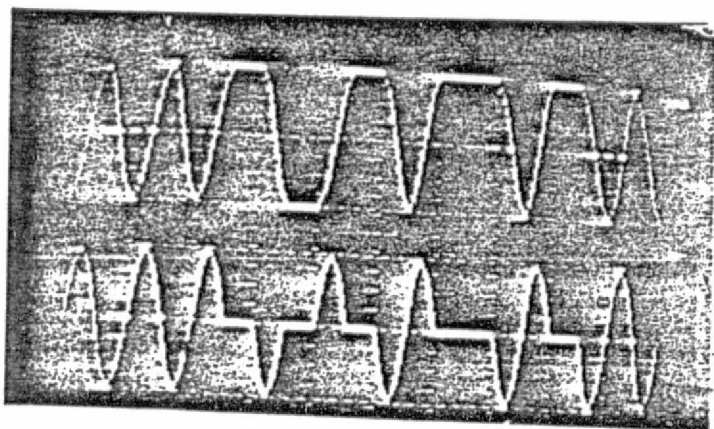
I&Q Data SMSK
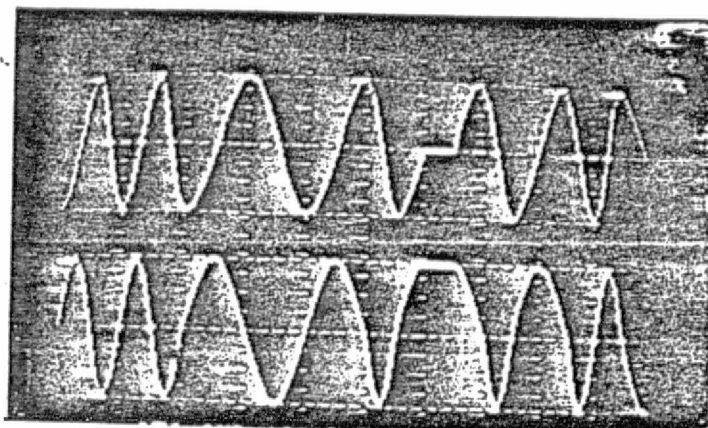
I&Q Data SMSK/2
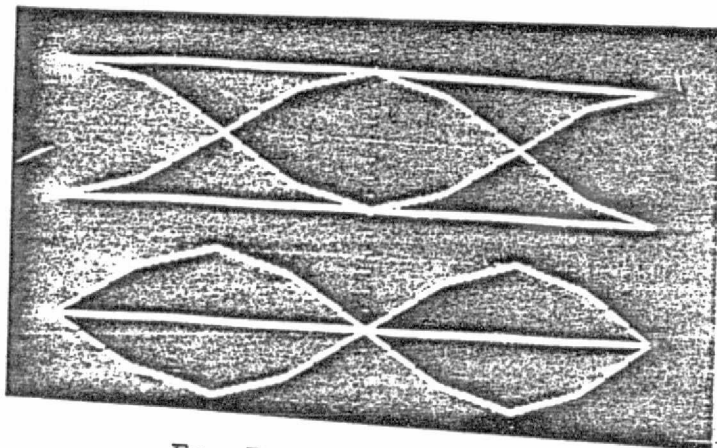
Eye Patterns SMSK
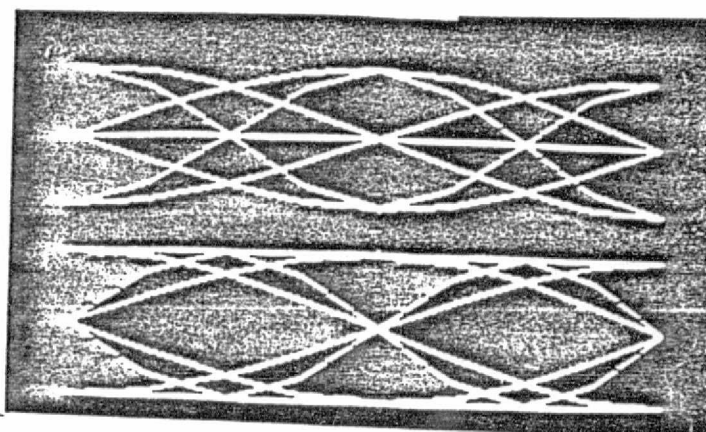
Eye Patterns SMSK/2
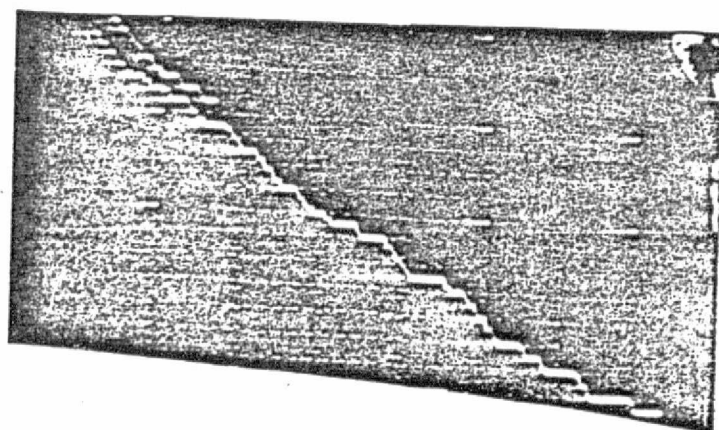
Excess Phase SMSK

Horz = 60T   Vert = (16)(2π)
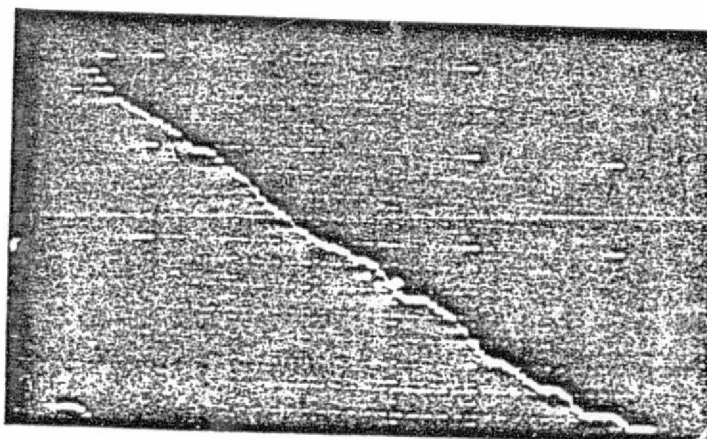
SMSK/2

Horz = 60T   Vert = 16x2π

Figure 3 provides a comparison between SMSK and SMSK/2. This figure illustrates the I and Q waveforms, the eye patterns, and the excess phase. The figure illustrates that the I and Q waveforms are similar except that the eye opening is multi level with an amplitude of 1.0 and .707. The excess phase curve for the SMSK/2 has less variation from the mean slope which indicates a reduction in bandwidth requirement over that of SMSK.

The SMSK/2 modulation has been configured such that it is suitable for implementation at very high data rates. Figure 4 illustrates the processing that must be performed. Two basic operations are included here, the first is the data coder/phase modulator and the second is the phase trajectory converter.

DATA CODER/PHASE MODULATOR

This portion of the modulator provides the necessary I and Q data inputs to the I/Q modulator to create a maximum of 90° phase transition per bit time. The data that is provided as inputs to the I/Q modulator is processed to make the I(t) signal approximate the Hilbert transform of the Q(t) signal, hence the entire unit approximates a single side band modulator.

PHASE TRAJECTOR CONVERTER

This portion of the modulator converts the phase steps obtained from the I/Q modulator to the phase trellis given in Figure 1. This is accomplished by using a cascade of two Filter-Limiter Networks. The filter is a single pole network
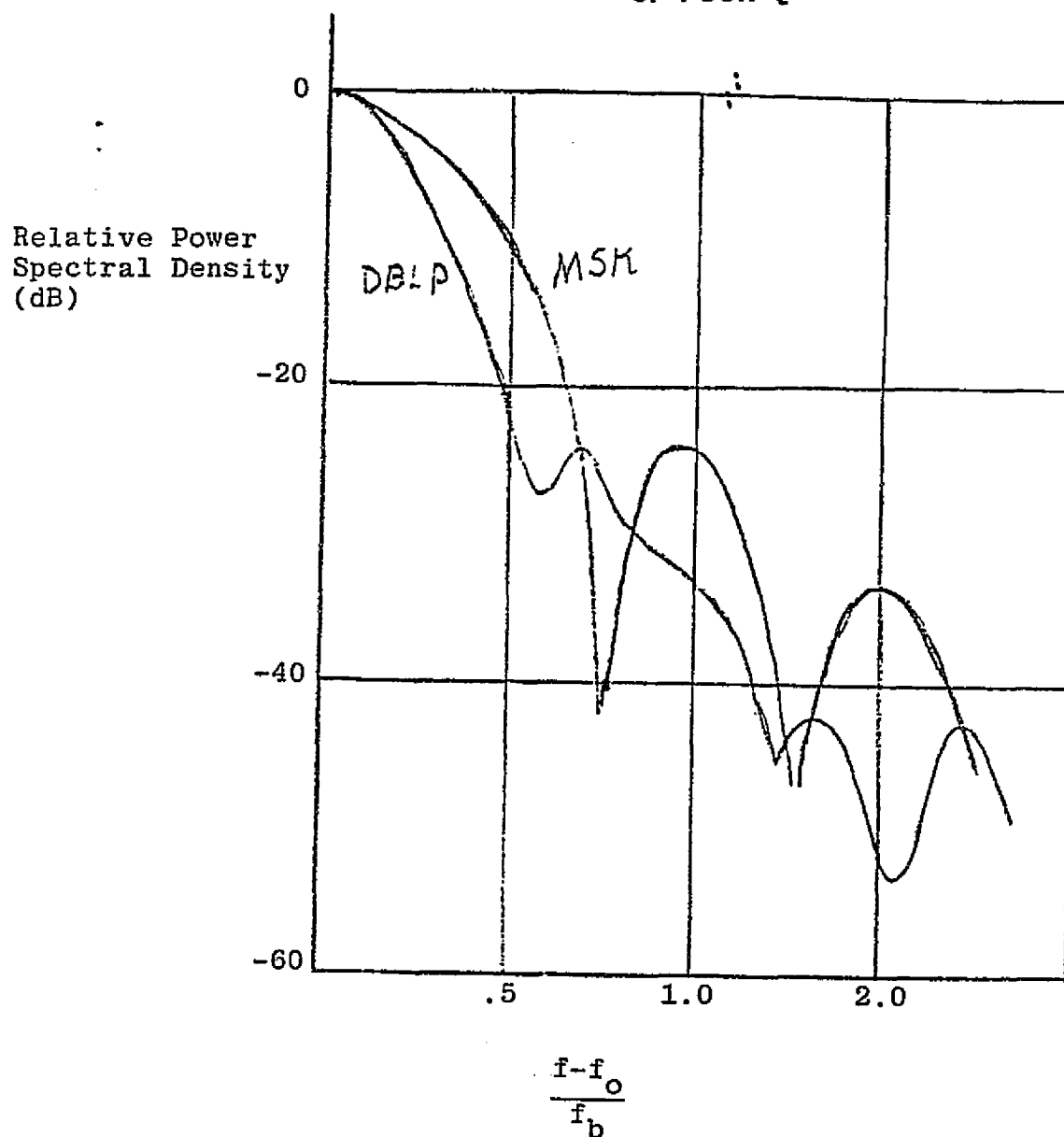
Figure 3   Power Spectral Density Comparison
of MSK and SMSK/2 (DBLP)

DATA CODER/PHASE MODULATOR

PHASE TRAJECTORY CONVERTER

DATA → ÷2 → ⊕ → I(t) / Q(t) → I/Q MODULATOR → BPF → ∫ → BPF → ∫ → BPF → OUTPUT

REFERENCE f₁
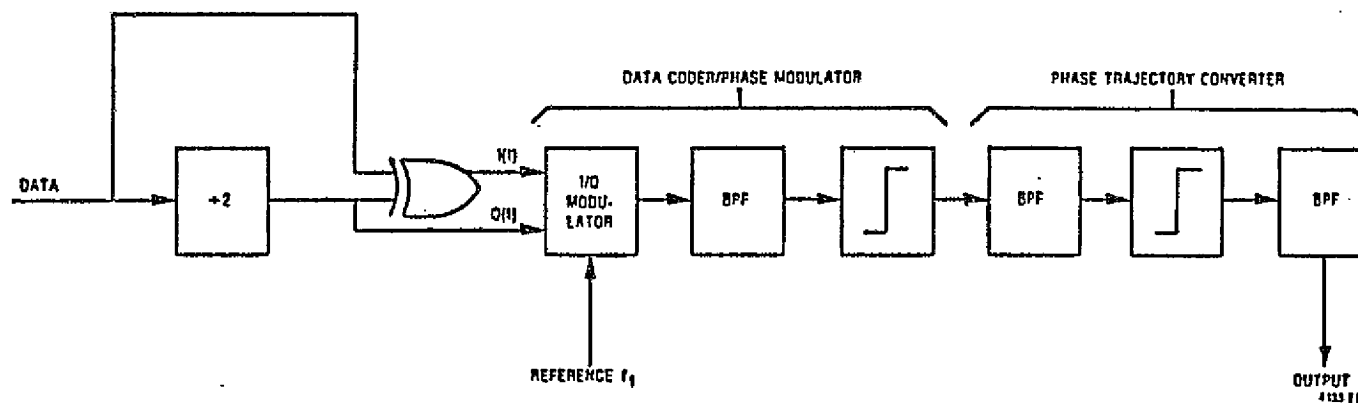
Figure 4   SMSK/2 Modulator

tuned to f_1 and has a bandwidth of R. This passband of the
Filter Limiters has been selected such that the desired
intergration of the phase steps is obtained.

TRANSMITTER PERFORMANCE

The output of the modulator after a 3 pole channel
filter with a 3dB bandwidth of 40 MHz is illustrated in
Figures 5 and 6.

DEMODULATOR

The demodulator consists of an I/Q phase detector and a
matched filter followed by a threshold detector and data
register (flip flop). This implementation is illustrated in
Figure 7.

The Detector EYE opening is a good measure of the
achievable performance. Figure 8 illustrates the measured
performance of this unit with a single pole "matched"
filter and indicates the potential performance obtainable
from this design.
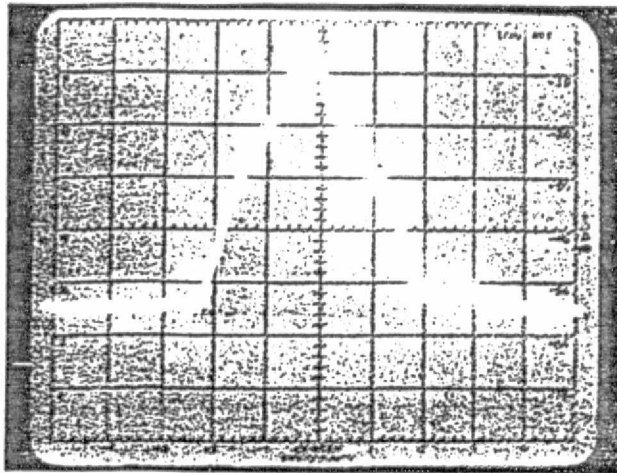
50 MB/S
10 dB/DIV HORIZONTAL
20 MHz/DIV VERTICAL
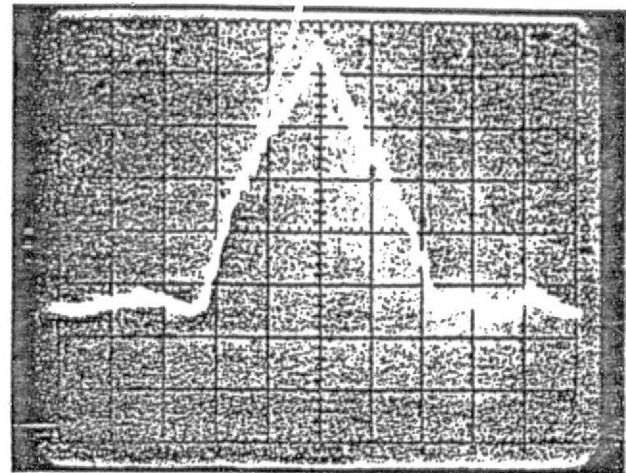
85 MB/S
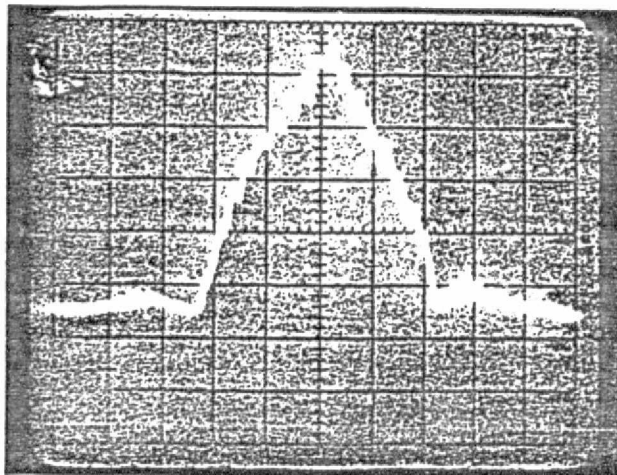
120 MB/S

4133-22

Figure 5   Transmitted Power Spectral Density
            R = 50, 85, and 120 MB/s
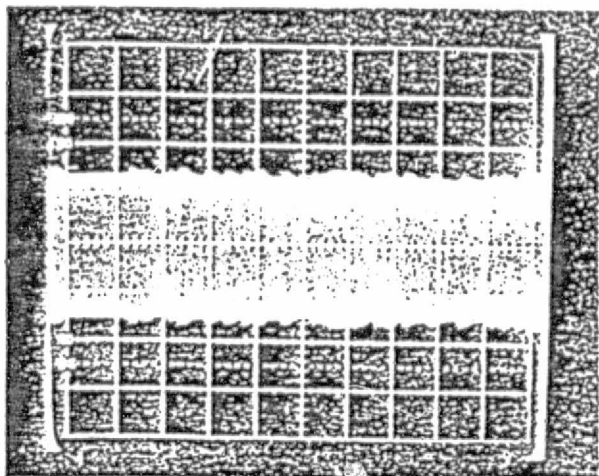
50 MB/S

50 NS/DIV HORIZONTAL
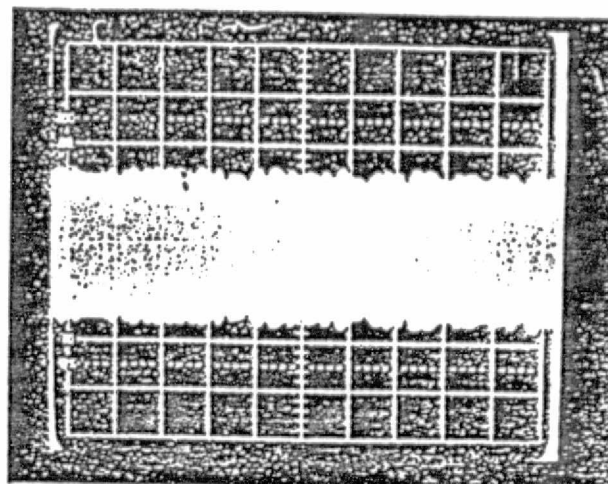
85 MB/S
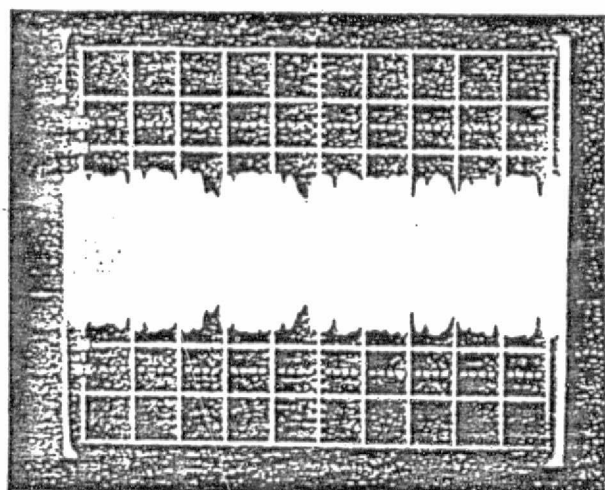
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OF POOR QUALITY

120 MB/S

4133-23

Figure 6   Output Envelope Amplitude for
50, 85, and 120 MB/s
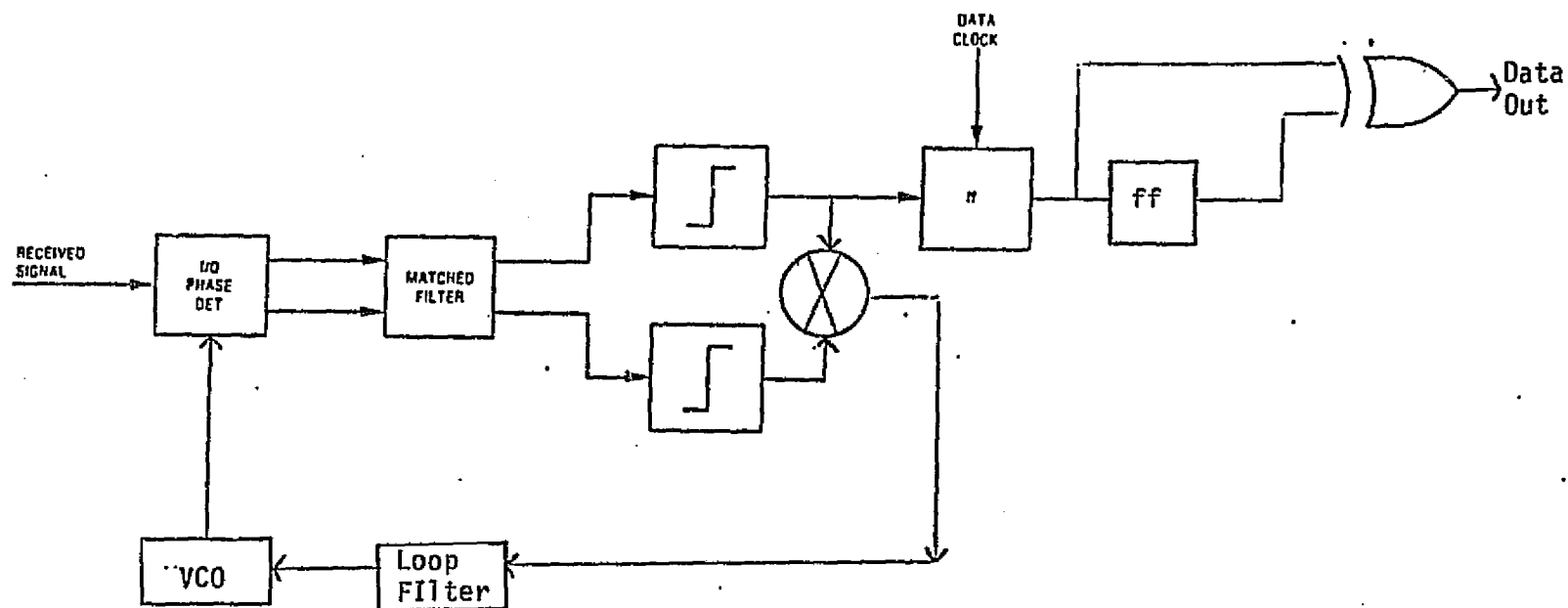
Figure 7   SMSK/2 Demodulator
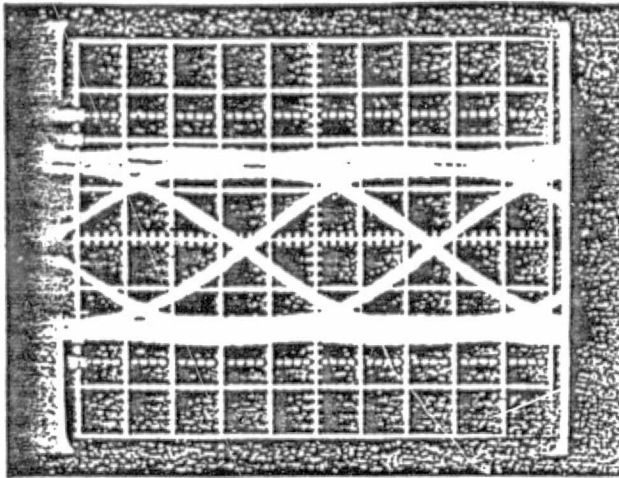
HORIZONTAL 5 NS/DIV
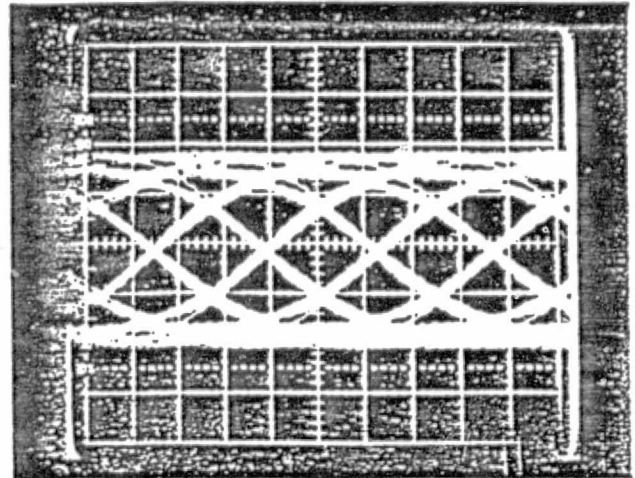
85 MB/S
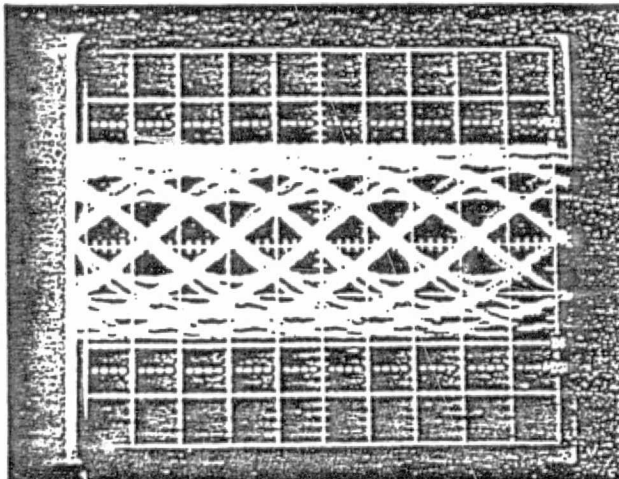
120 MB/S

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OF POOR QUALITY

4133-25

Figure 8   Demodulator Output After Channel
              Filter and Matched Filter

APPENDIX III

THRESHOLD DECODABLE CONVOLUTIONAL CODES
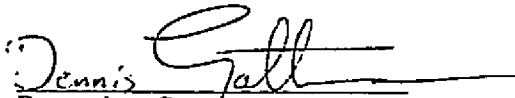
High Rate Threshold Decoding
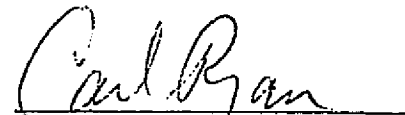
June 30, 1983

Presented to: LINCOM

Prepared by: *Dennis Gall*
Dennis Gottman
Communications Research
Facility

Approved by: *Carl Ryan*
Carl Ryan, Manager
Communications Research
Facility

HIGH RATE THRESHOLD DECODING

In order to obtain adequate link performance some sort of error correction coding will be required. Previously, threshold decoded block coding schemes and convolutional coding with Viterbi decoding have been considered. Also of potential interest are threshold decodable convolutional codes. Threshold decoding provides good performance characteristics with relatively simple implementation and therefore have lower development cost.

Majority-logic or threshold decoding is an algebraic approach to decoding of convolutional codes. It differs from Viterbi decoding and sequential decoding in that the final decision made on a given information block is based on only one constraint length of received blocks rather than on the entire received sequence. This results in inferior performance when compared to Viterbi or sequential decoding, but the implementation of the decoder is much simpler. An example coder and threshold decoder system for a (2,1,6) self-orthogonal code is shown in Figure 1.

Several high rate threshold decodable convolutional codes are currently in use. Table 1 summarizes the properties of four such codes. The performance characteristics of the two example rate 7/8 codes are shown in Figure 2[†]. These codes should provide adequate error correction capability with sign-ificant reduction in decoder complexity, as compared to the Viterbi algorithm.

[†] W.W. Wu, "New Convolutional Codes, Parts I – III", IEEE Trans. Commun., COM-23,24, Sept. 1975, Jan. 1976 and Sept. 1976.
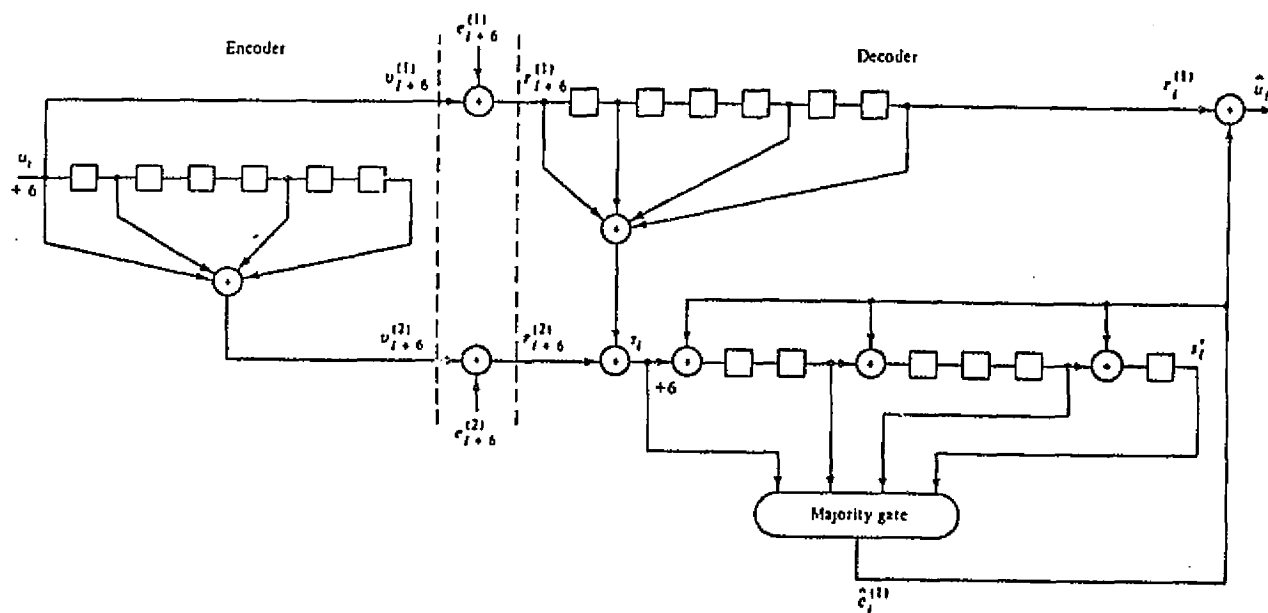
Figure 1 System Block Diagram for a (2,1,6) Self-Orthogonal
Code with Threshold Decoding

Table 1. High Rate CSOC's

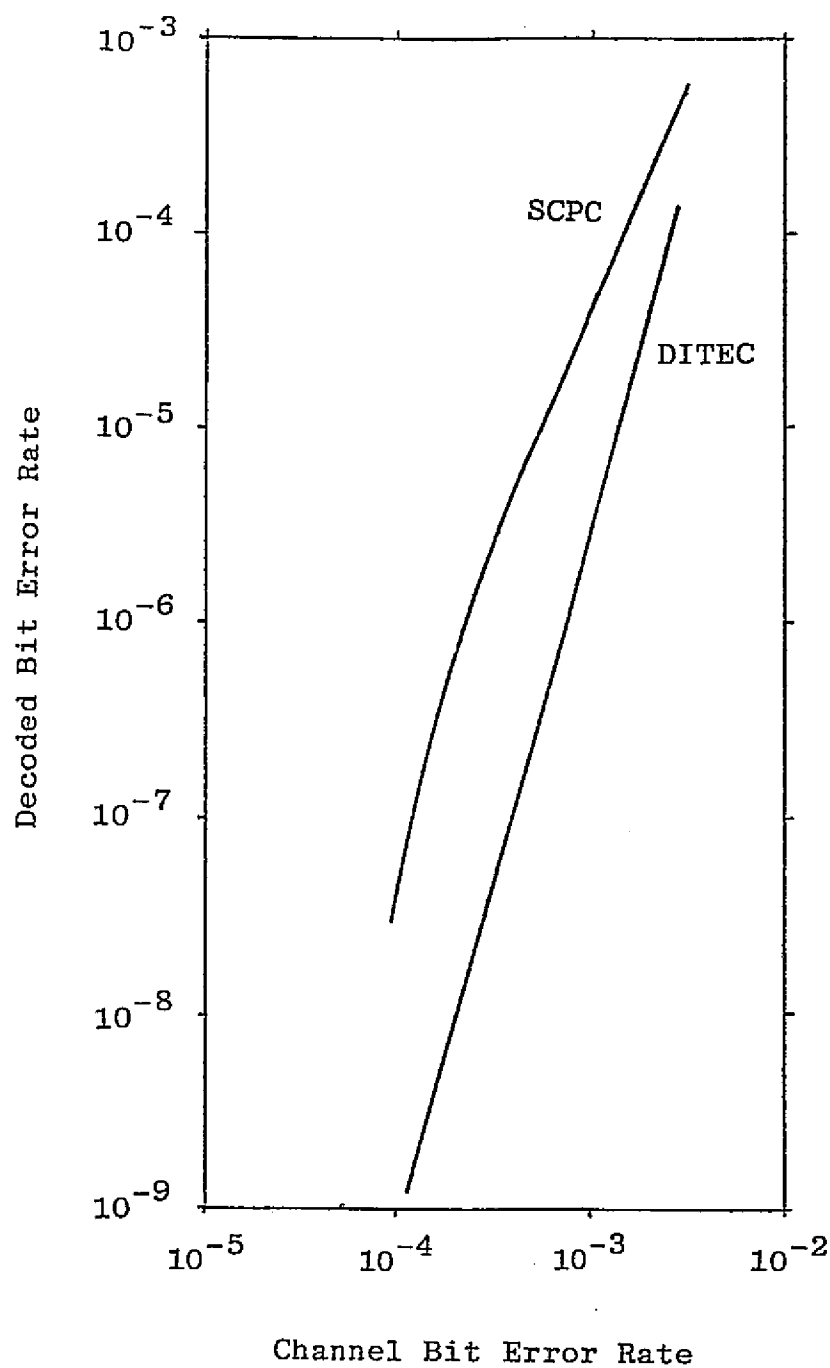|	Code Rate R	Constraint Length n_A	Effective Constraint Length n_e	Number of Syncrome Equations J	Minimum Distance dim
SPADE	3/4	80	31	4	5
INTELSAT SCPC	7/8	376	71	5	5
DITEC	7/8	1176	148	6	7
TDMA	8/9	1233	81	4	5

Figure 2a   Error Rate of Rate 7/8 Codes
            with Threshold Decoding
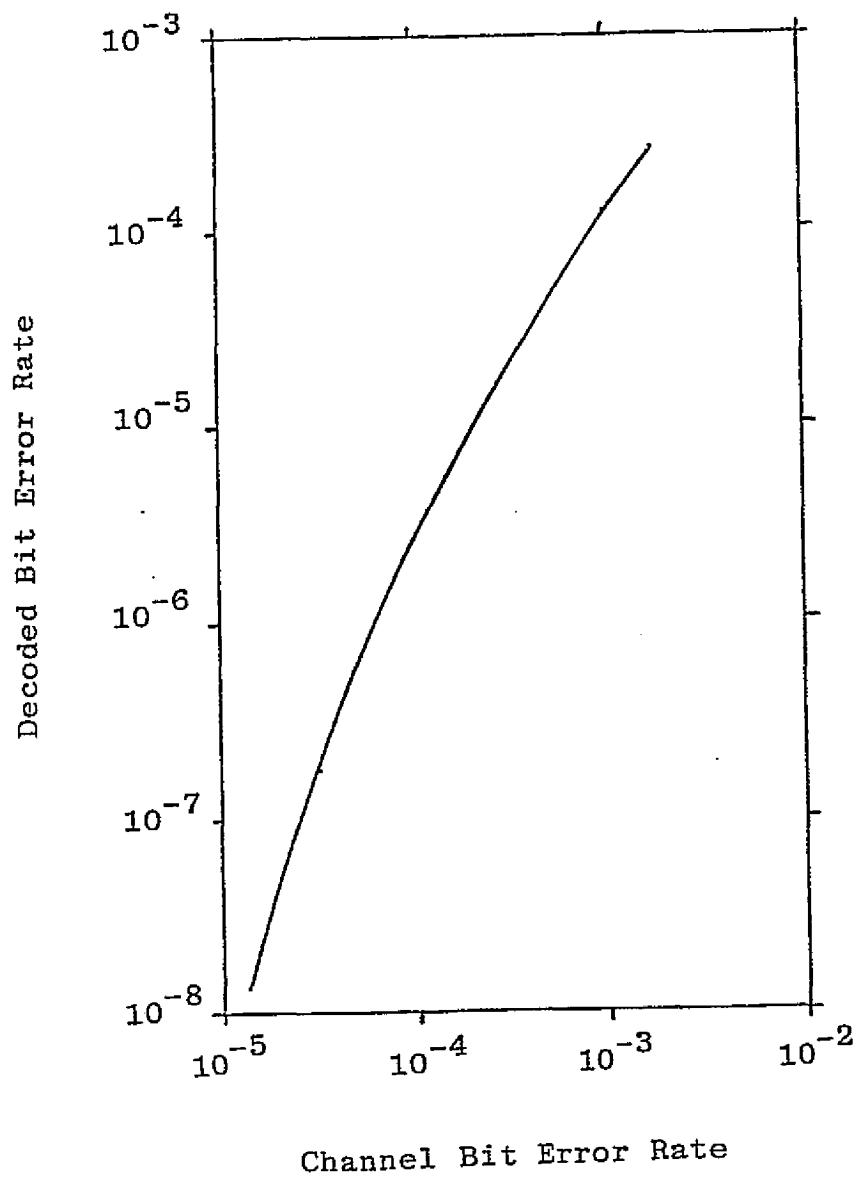
Figure 2b   Error Rate of Rate 8/9 Code (TDMA)
            with Threshold Decoding

These encoders can be implemented using a Type II coder, as described by Massey*. The general form is shown in Figure 3. The corresponding decoder is shown in Figure 4. At the data rate required in this application the multiplexers would need to be constructed using ECL elements, however, all of the coding and decoding logic could be implemented using TTL or CMOS circuitry. The rate 7/8 codes of Table 1 would require parts counts as indicated in Table 2. The feedback decoders will be approximately $2\frac{1}{2}$ times the complexity of the encoders.

There may also be effective ways of improving the threshold decoder performance by using soft data information. Potential schemes range from relatively simple to moderately complex. The simplest method would be to increase the threshold in the majority gate when a "strong" data bit is under consideration. This scheme would require approximately a 30% increase in decoder complexity. A more complicated system would retain the soft information at all points in the decoder. A possible exclusive - or replacement is shown in Figure 5. These more complex decoding schemes would nearly double the decoder hardware complexity.

As of now no analysis has been performed to indicate how much improvement can be had with any of these schemes. Even the most modest performance improvements might warrant the increase in decoder complexity since the original decoder is relatively simple. There remains a significant amount of work in determining the decoder structure and its performance characteristics.

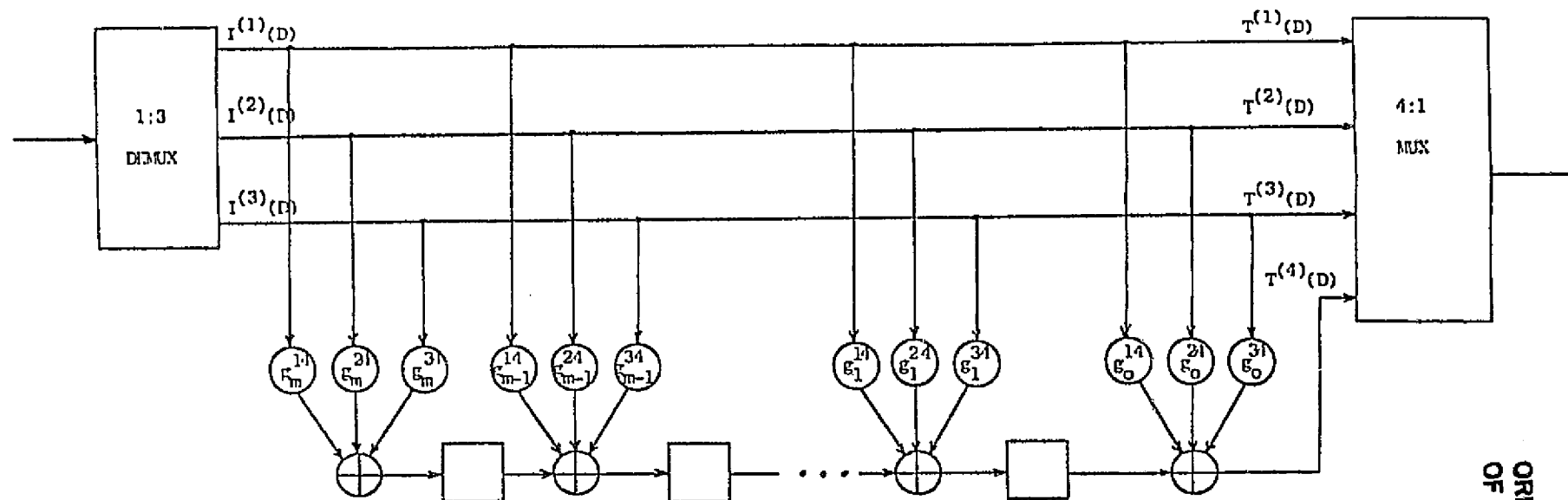* J.L. Massey, "Threshold Decoding", Cambridge, Mass, MIT, Press, 1963

Figure 3   General Form of Type II Massey Rate 3/4
Convolutional Encoder

Figure 4   Threshold Decoder for Rate 3/4 Encoder
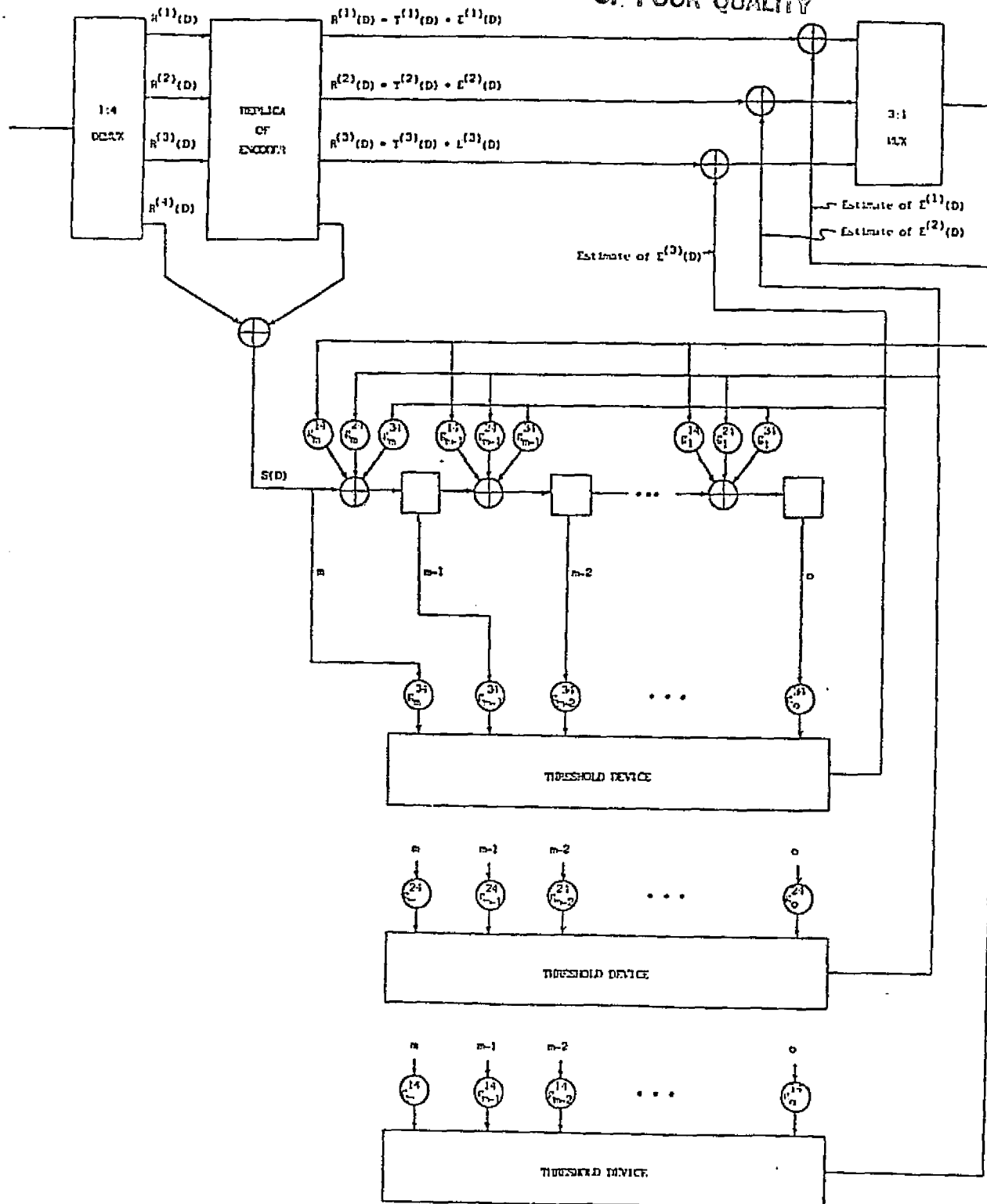of Figure 3

III-9

Table 2.   Rate 7/8 Coder TTL Parts Count

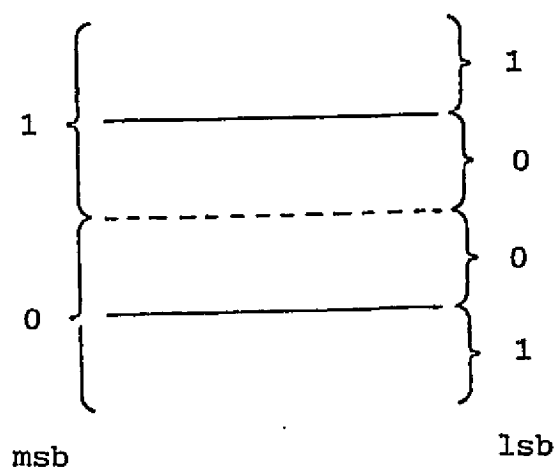| Code	TTL Parts Count		
	74164	74280	74386
SCPC	6	1	4
DITEC	19	1	7

Figure 5a Soft Decision Threshold Levels

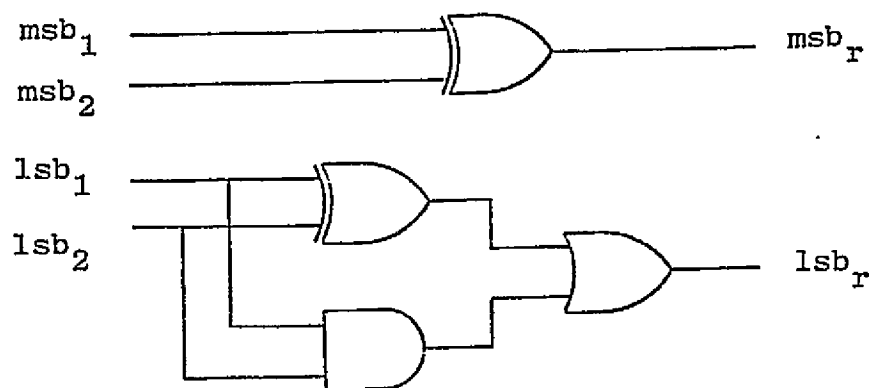Figure 5b Possible Configuration of a "Soft EOR"

At this point there remains a substantial amount of work
to be done in selecting an appropriate coding scheme. One
fundamental concern is an accurate estimate of the coding gain
required for adequate system performance. Once this is obtained
the selection of a coder/decoder structure can be finalized.
The two rate 7/8 codes and possibly the rate 8/9 code discussed
previously should be prime candidates to fulfill this system
need. These coding structures provide significant error cor-
rection capabilities and are relatively simple to implement.
There may also be ways of further improving performance through
the use of soft decisions in the decoding algorithm while main-
taining a relatively simple hardware implementation. In all,
threshhold decoding of convolutional codes is a very attractive
alternative and warrants careful consideration.

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APPENDIX IV

MOTOROLA SMSK/2 DETAILED COST ESTIMATE

LinCom

MOTOROLA INC.

COMMUNICATIONS RESEARCH FACILITY
TECHNICAL MEMO

Estimated Satellite Data Modem Follow-On Activity

17 November 1983

Prepared by:

Carl Ryan, Manager
Communications Research Facility
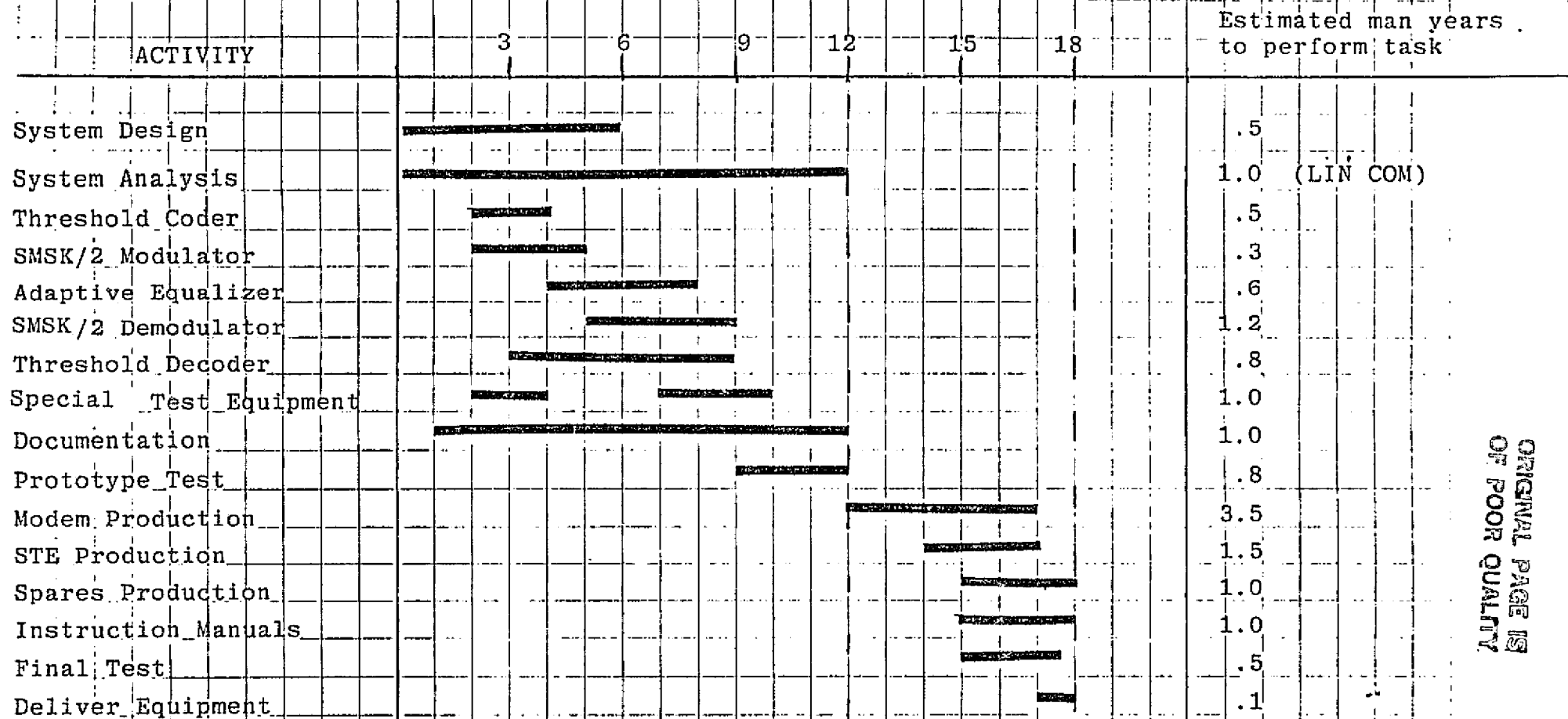(602)892-2100

Satellite Data Modem Follow-On Activity

The follow-on activity required to complete the development and production of two full duplex modems, special test equipment and spare parts is indicated in this report.

The following deliverable items are included in this estimate.

1. Two full duplex modems each consisting of:

   a) modulator

   b) encoder

   c) equalizer

   d) demodulator

   e) decoder

2. Two sets of special test equipment required for maintaining the equipment

3. Two sets of spare parts and replaceable subassemblies

4. Instruction manuals for operation and maintance of the equipment

The schedule for the follow-on activities is illustrated in Figure 1 and is based on a 12 months developmental effort and a 6 month production cycle for a total of 18 months to delivery of the equipment. Included in Figure 1 is the estimated man years required to accomplish each task. The total man years required during the development phase which would result in a operational prototype is approximately 7.7. The production phase will require 7.6 man years for a total of 15.3 man years of effort.

Figure 1 Satellite Data Modem Schedule

ACTIVITY	Schedule (months: 3, 6, 9, 12, 15, 18)	Estimated man years to perform task
System Design		.5
System Analysis		1.0 (LIN COM)
Threshold Coder		.5
SMSK/2 Modulator		.3
Adaptive Equalizer		.6
SMSK/2 Demodulator		1.2
Threshold Decoder		.8
Special Test Equipment		1.0
Documentation		1.0
Prototype Test		.8
Modem Production		3.5
STE Production		1.5
Spares Production		1.0
Instruction Manuals		1.0
Final Test		.5
Deliver Equipment		.1

PHASE DEVELOPMENT ____ PRODUCITON PHASE

APPENDIX V

SDT LinCsim DESCRIPTION

APPENDIX V

ANALYTICAL SIMULATION

LinCom has performed an analytical simulation of the SDT communication system, as described in the LinCom/Motorola proposal [1]. The simulation models alternative SDT system configurations in software, so that various modulation/coding schemes can be compared against each other.

Several different channels were modeled in the simulation, and different groups of modulation/coding schemes were evaluated for each channel. In the first section of this appendix, a channel whose HPA and TWTA have the same nonlinear, saturating gain characteristic is used to compare the performance of the QPSK, 8PSK, and 16PSK modulations. 8PSK is further analyzed in Section 2 as channel parameters are changed. In Section 3, the performance and out-of-band power of 8PSK are compared against those of a simplified version of Motorola's DBLP modem on the revised model of the SDT channel.

1. Comparison of QPSK, 8PSK, and 16PSK Modulation Schemes

In the first phase of the simulation effort, LinCom compared the link performance of three different MPSK modulation schemes (M = 4,8, and 16) as various SDT channel parameters were changed. Both the uplink and downlink were included in the simulation model of the system (Figure 1). Modem simulation was emphasized over codec simulation, because the coding gain of commercially available codecs is well documented. Coding increases the symbol flow rate through the channel by the inverse of the code rate:

$$\text{Symbol Flow Rate} = \text{Data Bit Rate} \times (1/\text{Code Rate}) \qquad (1)$$
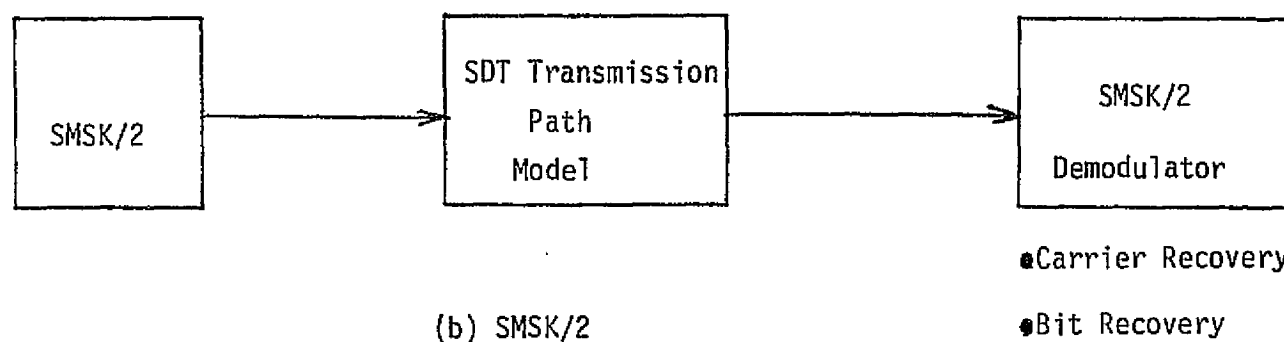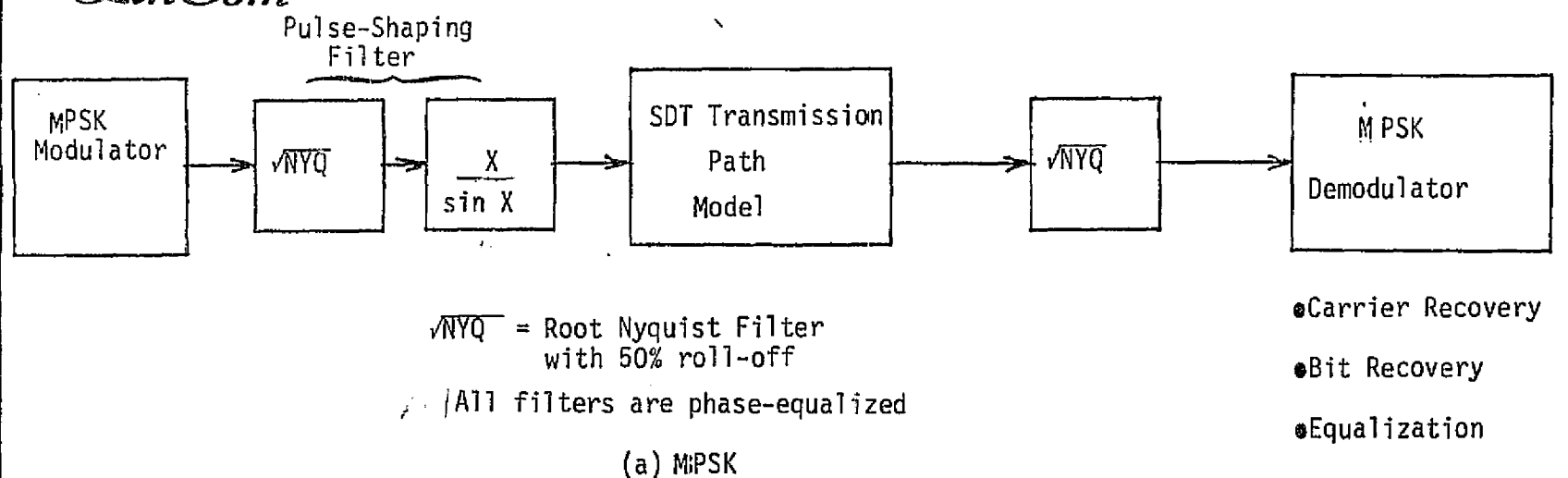
Figure 1.   MPSK and SMSK/2 Simulation Block Diagram

Table I.   Simplified Simulation Model for Satellite Transmission
            Path.

ITEM	MODEL
TRANSMIT CHANNEL FILTER ①	W = 38 MHz, 4-POLE*
HPA ②	INPUT BACKOFF 0-12 dB**
HPA OUTPUT FILTER ③	W = 38 MHz, 4-POLE*
SATELLITE CHANNEL FILTER ④	W = 34 MHz, 6-POLE*
TRANSPONDER TWTA ⑤	INPUT BACKOFF (AROUND 3 dB) TO BE OPTIMIZED**
TWTA OUTPUT FILTER ⑥	W = 34 MHz, 3-POLE*
RECEIVE CHAIN FILTER ⑦	W = 38 MHz, 4-POLE*

NOTES: * Chebyshev Filter, ideally equalized with 1 dB
             ripple and 3 dB RF bandwidth W.

           **See Figure 2 for AM/AM and AM/PM characteristics model.

In addition to the symbol rate, the delay equalization in the receiver is an important element of system performance. Although all filters in the system are assumed to be phase-equalized (Table I), the 1-dB peak-to-peak ripple of the Chebyshev filters accumulates in the channel to cause intersymbol interference (ISI). The nonlinear characteristic of the HPA and TWTA (Fig. 2) also contributes to the cumulative ISI in the receiver. Tapped delay-line equalization mitigates the receiver ISI, even when the number of taps is 3 or 5 (Figures 3 and 4, respectively).

Thermal noise and adjacent channel interference (ACI) also degrade the SDT link performance. LinCom modeled ACI and the uplink and downlink thermal noise as three independent additive white Gaussian processes in the SDT analytical simulation. This assumption permits simulation of almost all of the SDT communication system (Fig. 1). Analysis was performed only in deriving the channel symbol error rate at the demodulator.

In the absence of any coding, the symbol error rate is also the bit error rate by (1). An 85 Mbps QPSK modem without coding was simulated for the case where the HPA and TWTA are linear with no backoffs (i.e., the HPA and TWTA are ignored) (Figure 5). The bit error rate is larger than 10^{-4} even in this case; for nonlinear amplifiers, link performance is even worse (Figure 6). These results are primarily due to the low one-sided BT product (<0.5) for the channel, which means much of the signal power is filtered.

The BT product can be effectively increased by increasing the number of modulated bits per symbol transmission. Provided the bit rate does not rise significantly, we can thereby increase the symbol
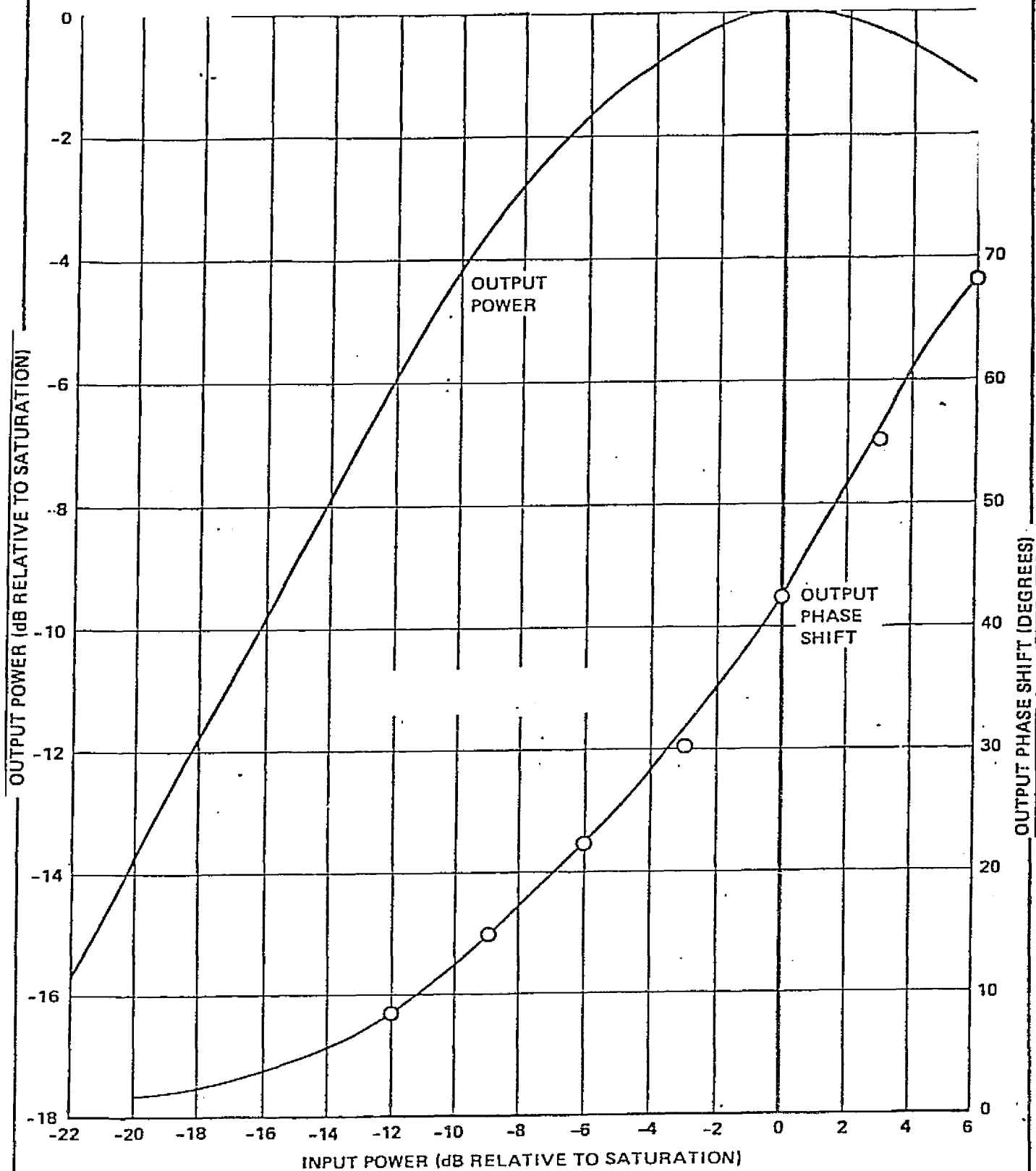
Figure   2.   Model Nonlinear Amplifier Input-Output Characteristics.
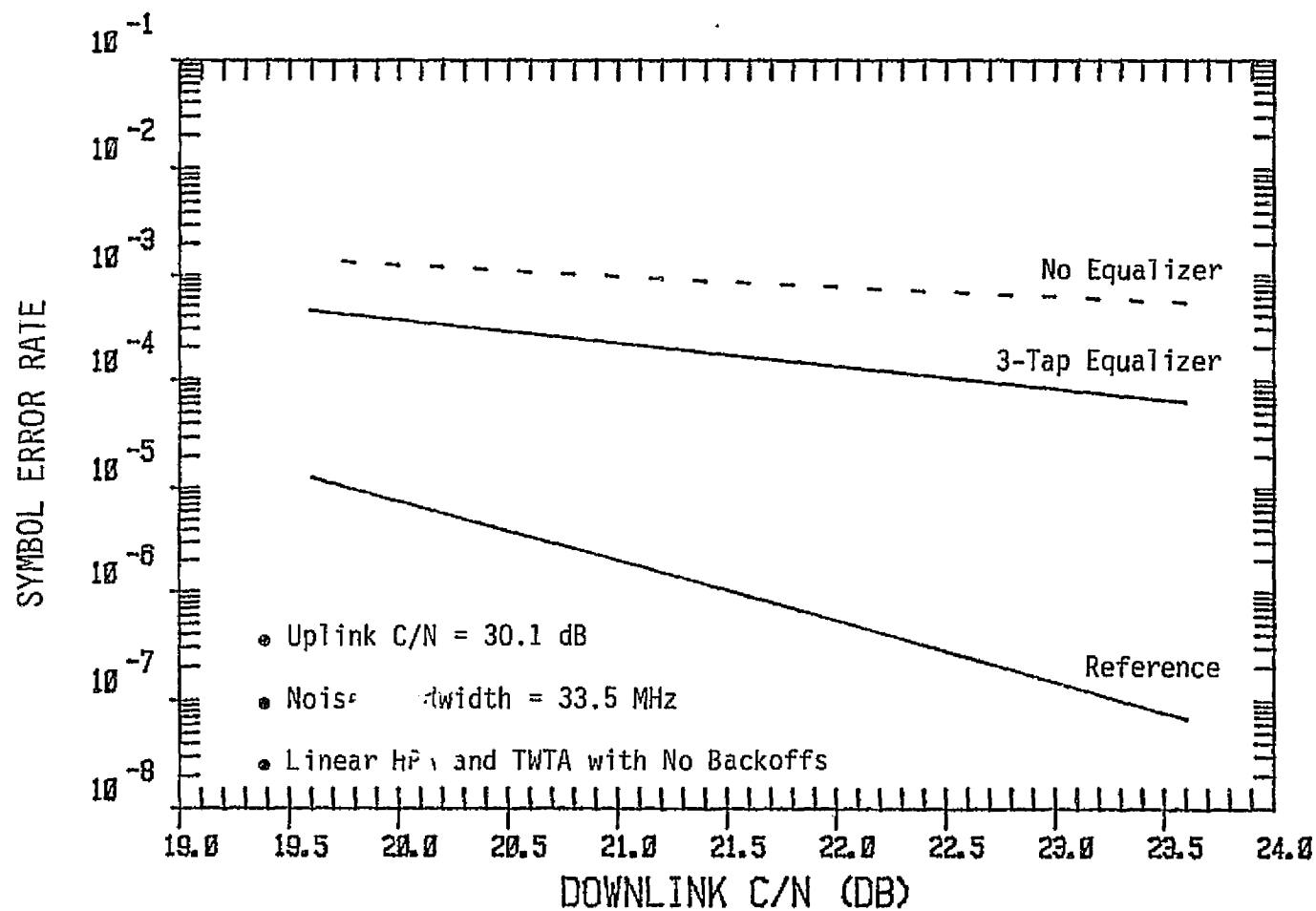
Figure 3.   Simulated Performance of 8PSK at 97.1 Msps (85 Mbps with Rate 7/8 Coding)
with 3-Tap Equalization.
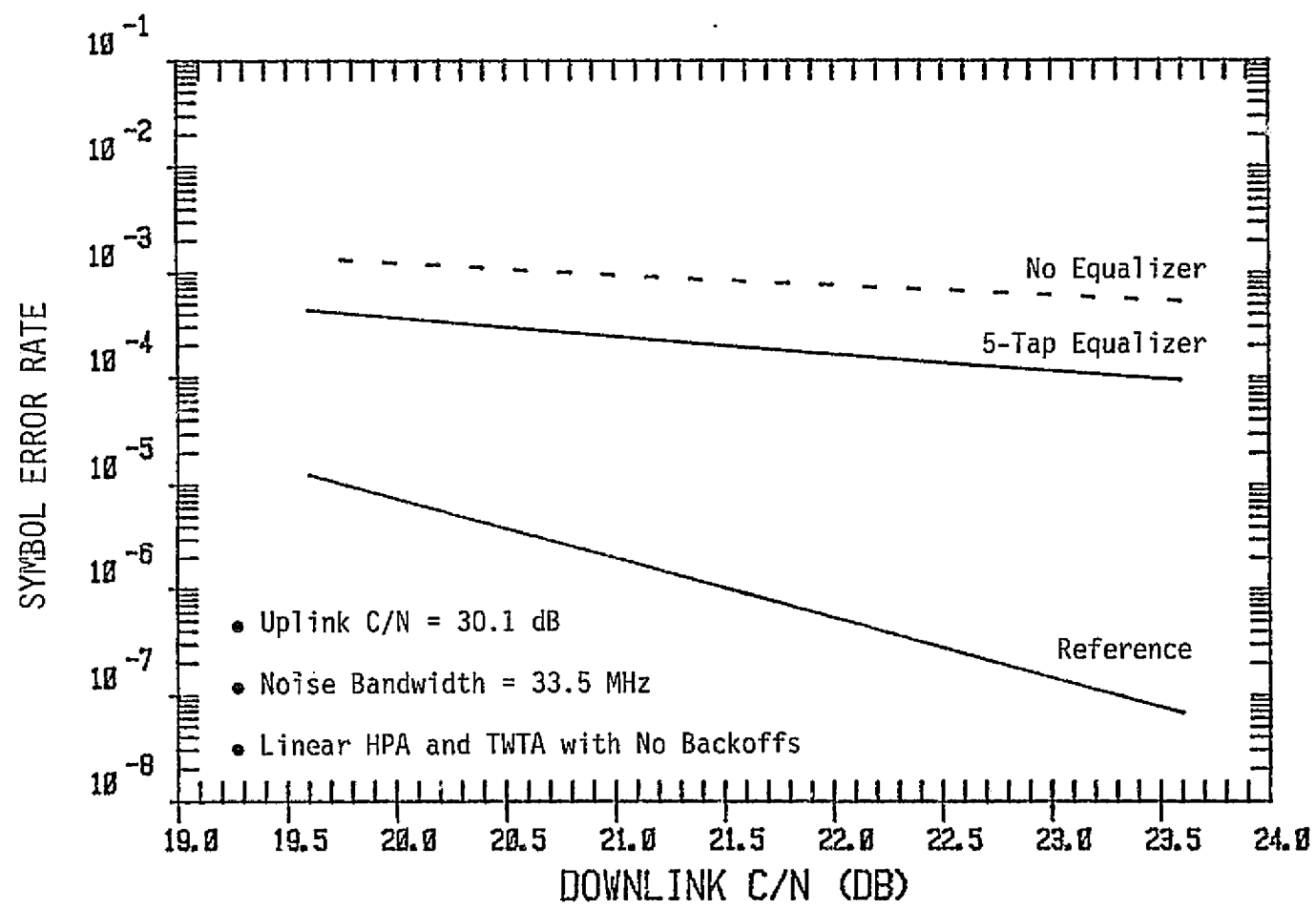
Figure 4.   Simulated Performance of 8PSK at 97.1 Msps
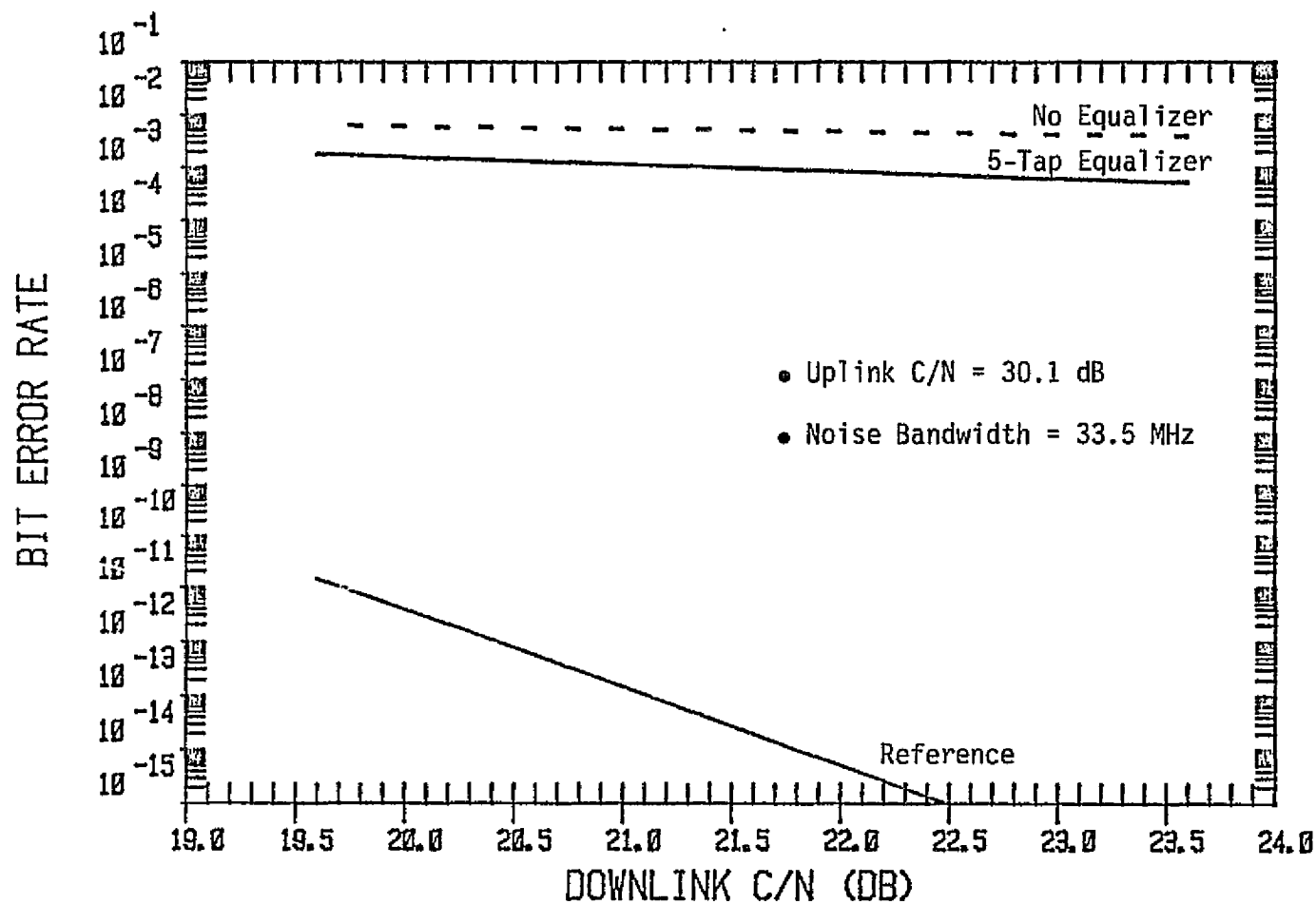   with 5-Tap Equalization

Figure 5. Simulated Performance of QPSK at 85 Mbps
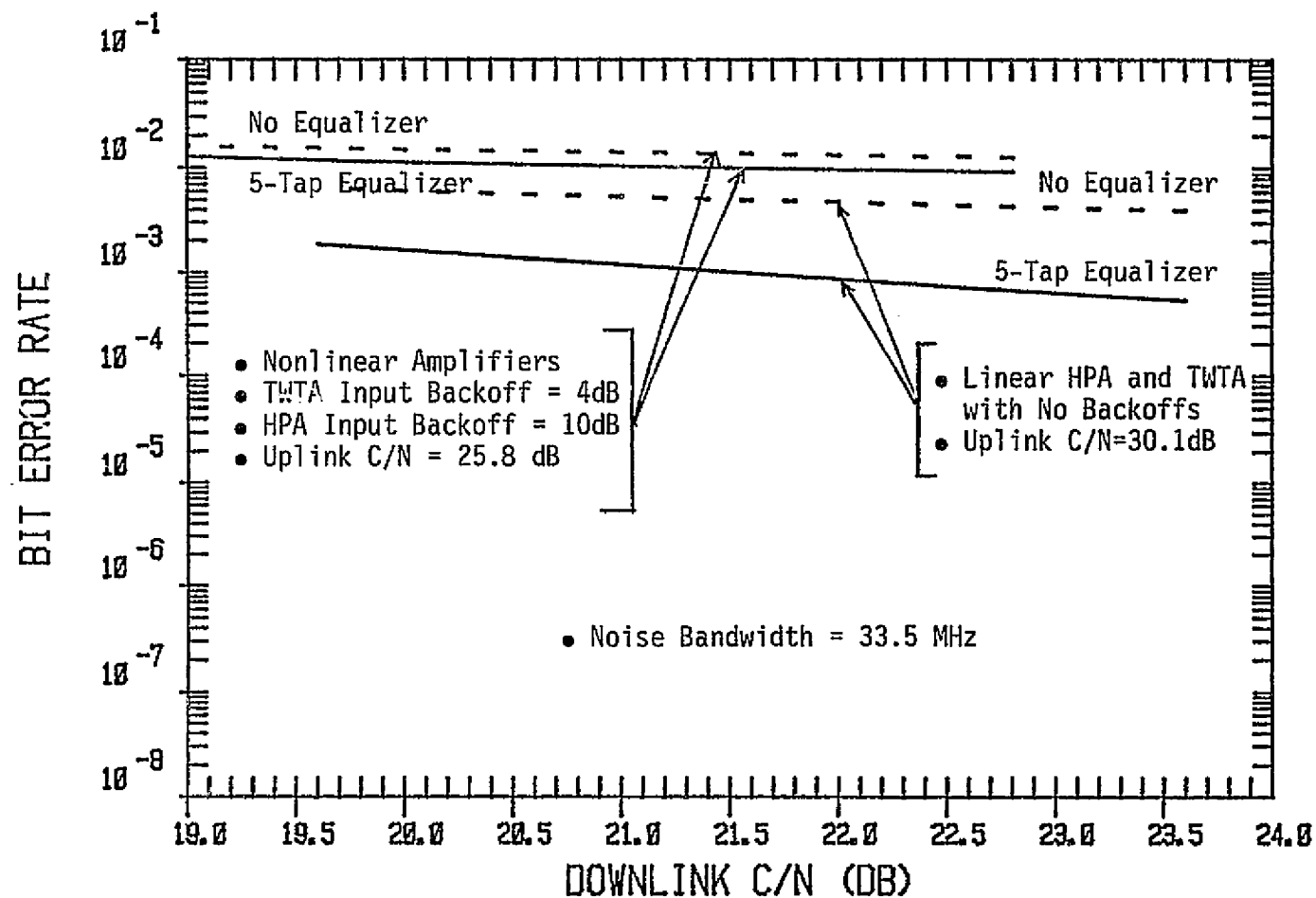Without Coding in a Linear Channel with No Backoffs

Figure 6. Simulated Performance of QPSK at 85 Mbps
Without Coding

transmission period T. 8PSK and 16PSK are two modulations which increase BT in this way. 8PSK has 8 modulated bits per symbol period T and 16PSK has 16, compared to just 4 for QPSK.

Although 8PSK and 16PSK are less susceptible to channel bandwidth constraints than QPSK, they are more sensitive to ACI and thermal noise. 16PSK is particularly vulnerable to these link conditions, because the separation between signal phases ($\pi/8$) is only half that of 8PSK. 16PSK and 8PSK performance are plotted for four different TWTA backoff conditions at 97.1 million coded symbols per second (Msps) in Figures 7 and 8, respectively. 97.1 Msps corresponds to 85 Mbps with rate 7/8 coding by equation (1).

Figures 6 through 8 shows that 8PSK performs better than 16PSK or QPSK at 97.1 Msps. QPSK is plotted in Fig. 6 with no coding; its performance will be even worse when coding is included. Of the three MPSK modems considered, 8PSK appears to offer the best tradeoff between bandwidth conservation and noise and interference immunity.

8PSK performance on the SDT link was investigated further. Figure 9 shows the sensitivity of the link performance to the HPA and TWTA backoffs. Since the lowest symbol error rate occurs near 8-dB TWTA input backoff, this value was chosen to show how 8PSK performance depends on HPA backoff (Figure 10). The sensitivity of 8PSK to the HPA and TWTA backoffs is slightly different for 3-tap equalization (Figure 11) and uncoded 8PSK (Figure 12).

2. Effect of Channel Modification on 8PSK Performance

Several changes were made in the SDT channel model (Fig. 2-1) after the three MPSK modulations were compared. 8PSK performs better than 16PSK or QPSK even in the new channel, because none of the modifications
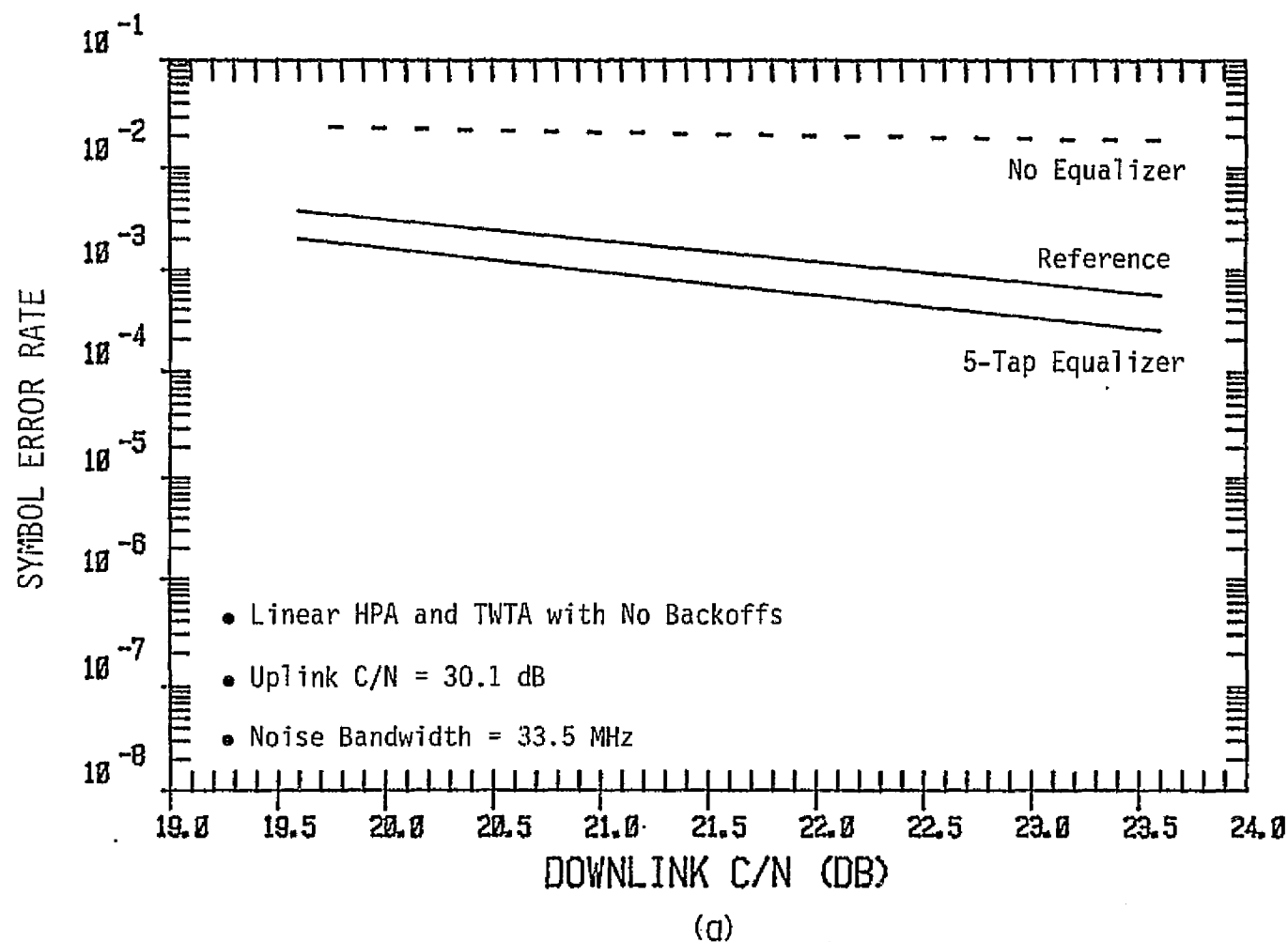
Figure 7. Simulated Performance of 16PSK at 97.1 Msps
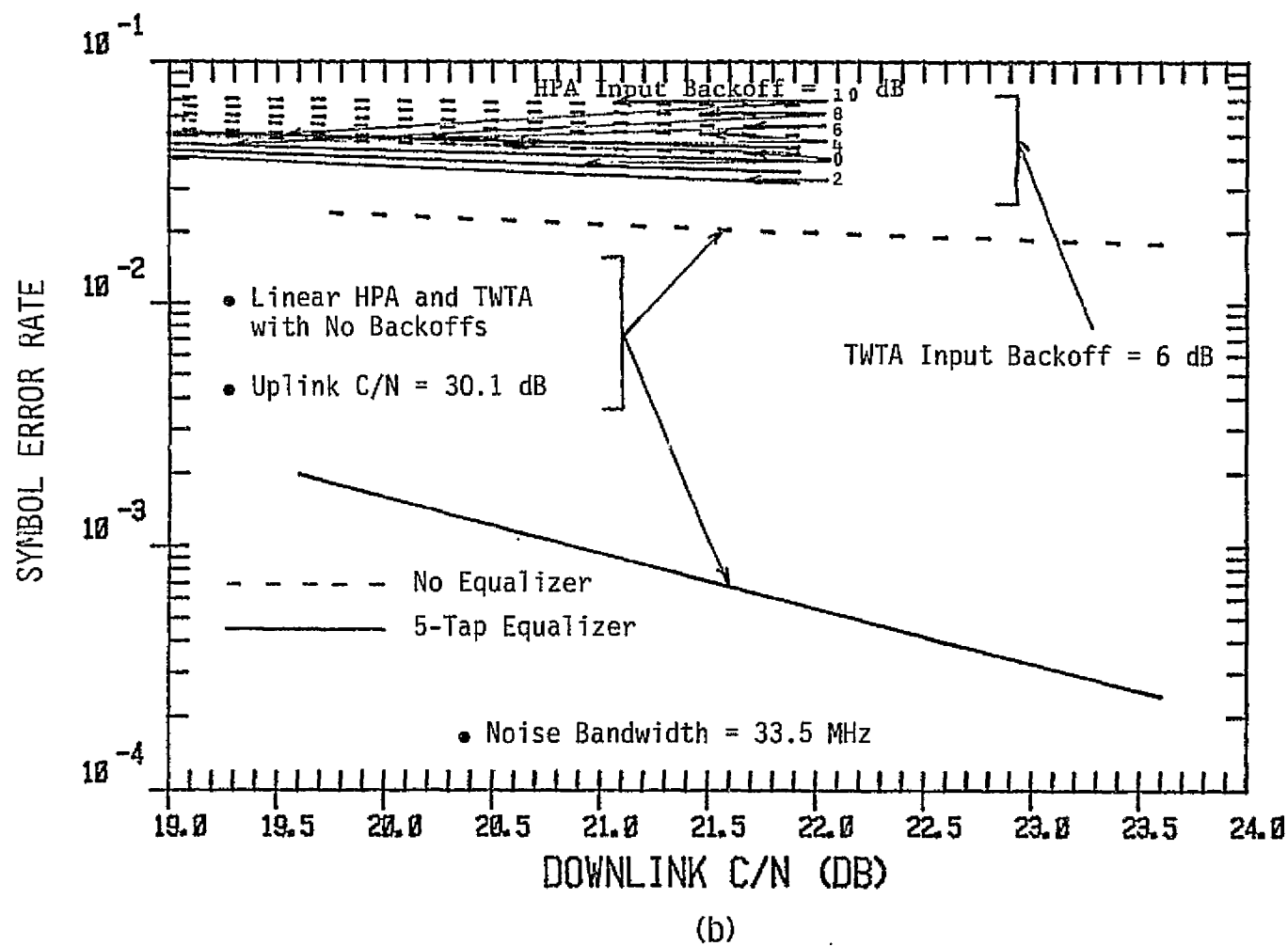
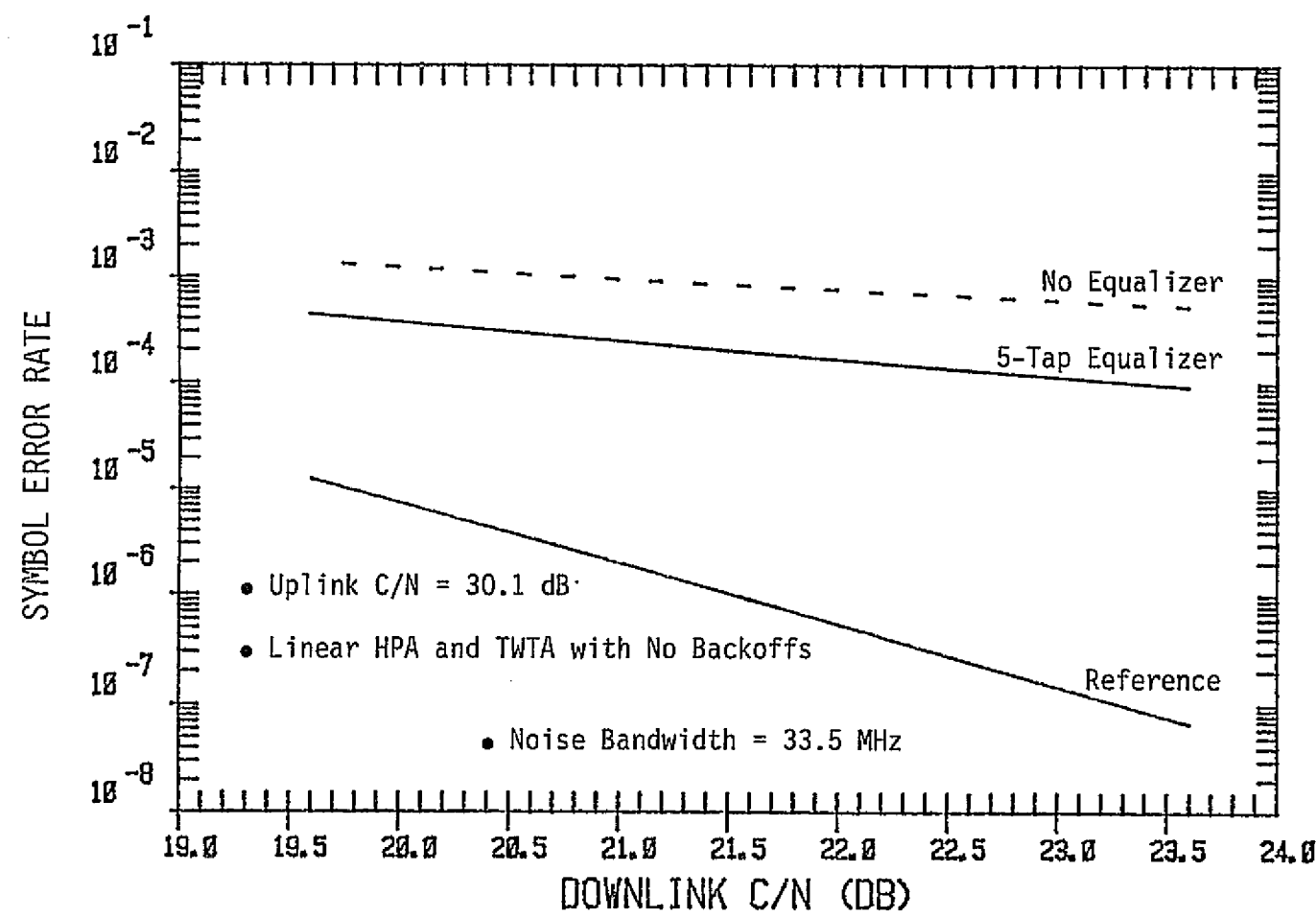Figure 7. Simulated Performance of 16PSK at 97.1 Msps

Figure 7. Simulated Performance of 16PSK at 97.1 Msps

Figure 7.   Simulated Performance of 16PSK at 97.1 Msps

Symbol Error Rate vs Downlink C/N (DB)

- Uplink C/N = 30.1 dB
- Linear HPA and TWTA with No Backoffs
- Noise Bandwidth = 33.5 MHz

No Equalizer

5-Tap Equalizer

Reference

(a)
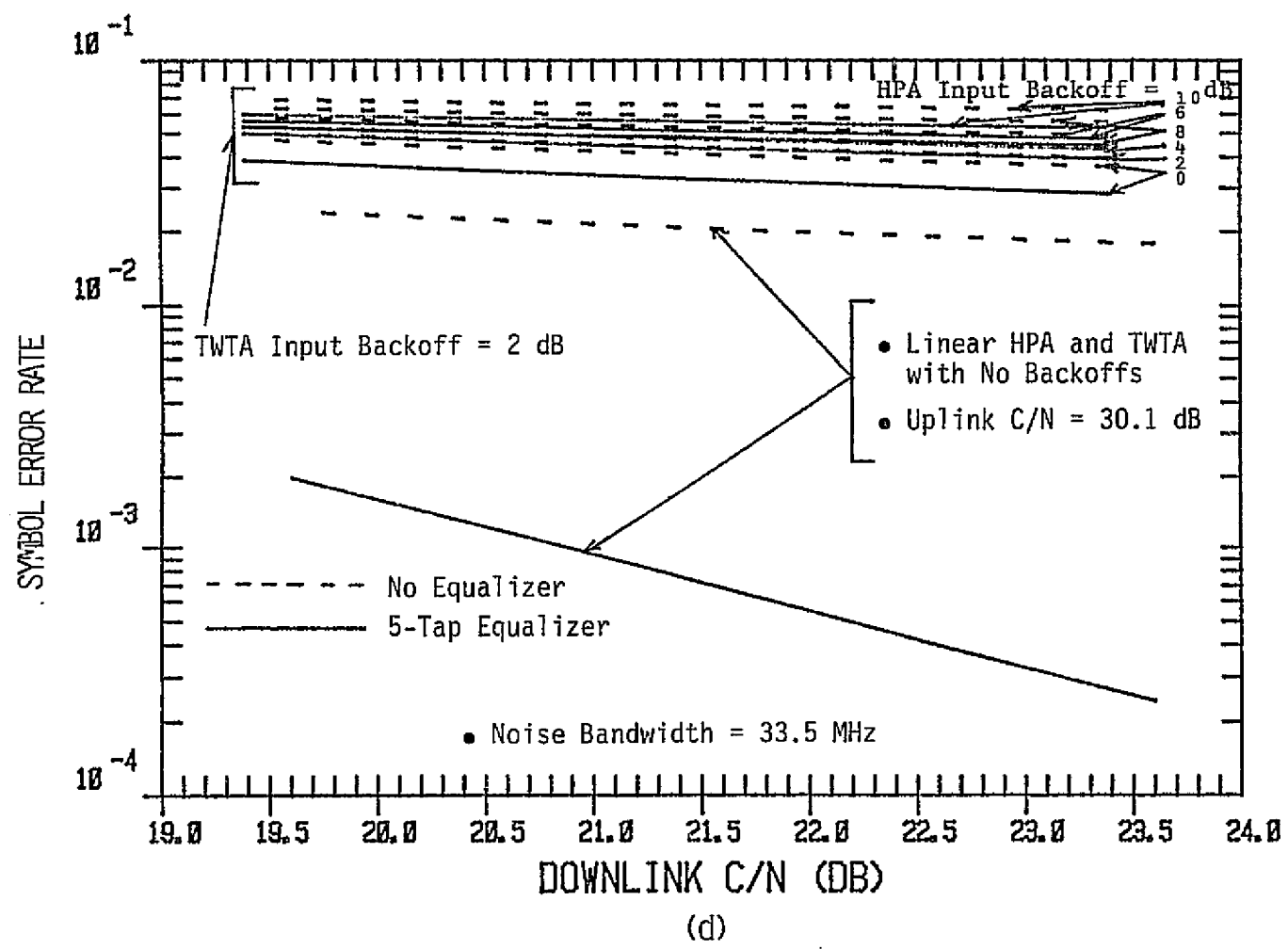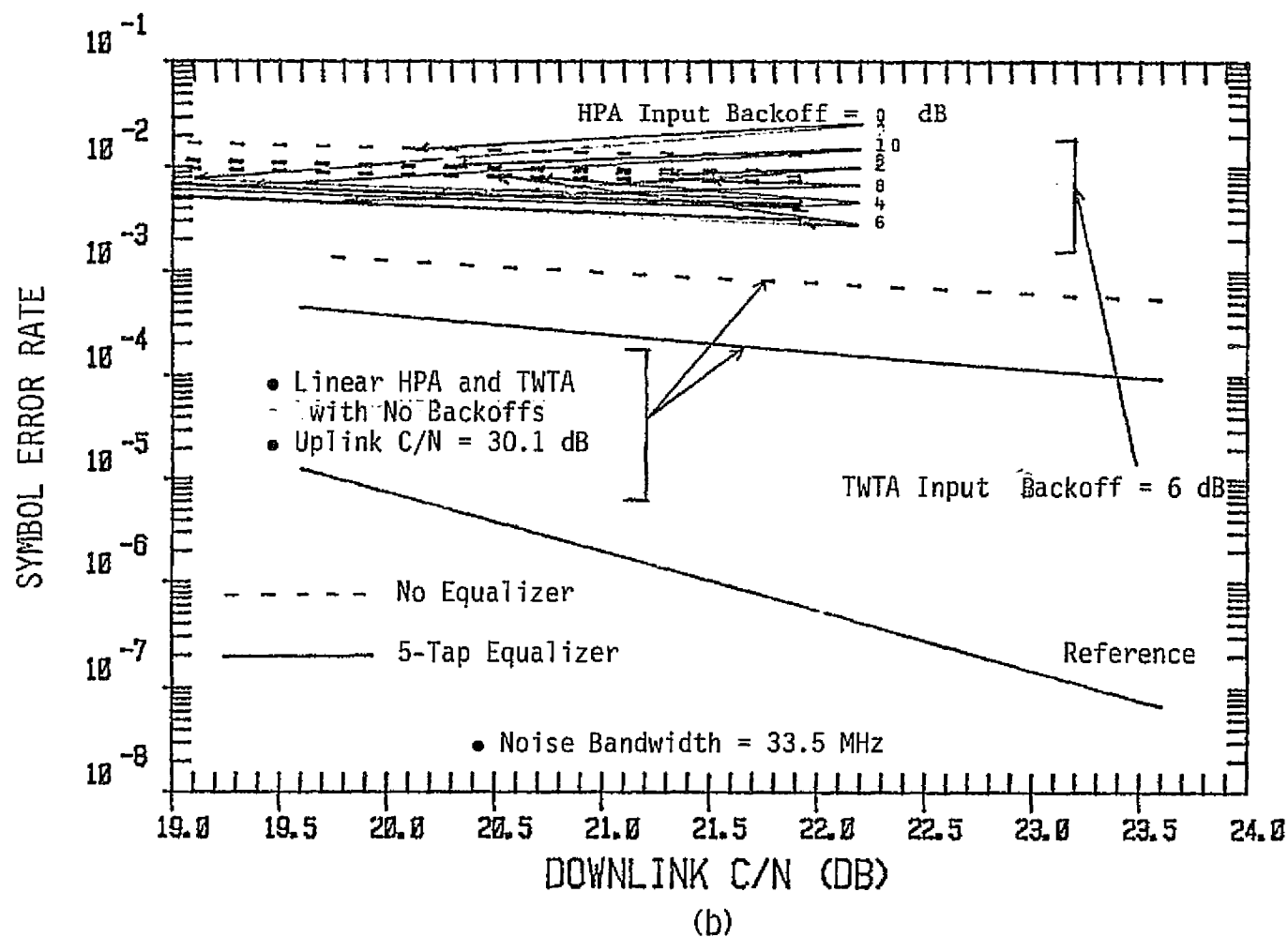
Figure 8.   Simulated Performance of 8PSK at 97.1 Msps
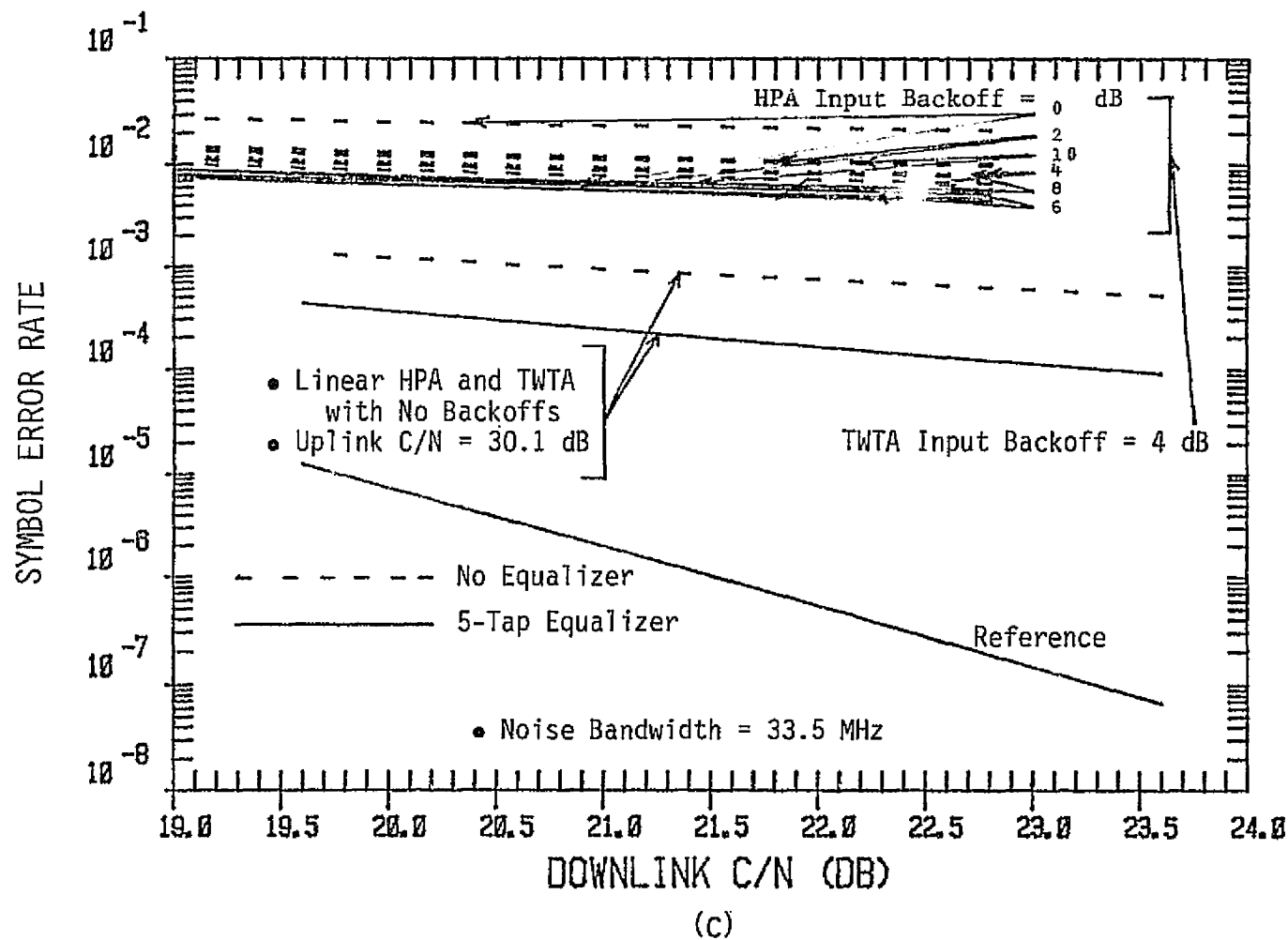
Figure 8. Simulated Performance of 8PSK at 97.1 Msps

Figure 8. Simulated Performance of 8PSK at 97.1 Msps
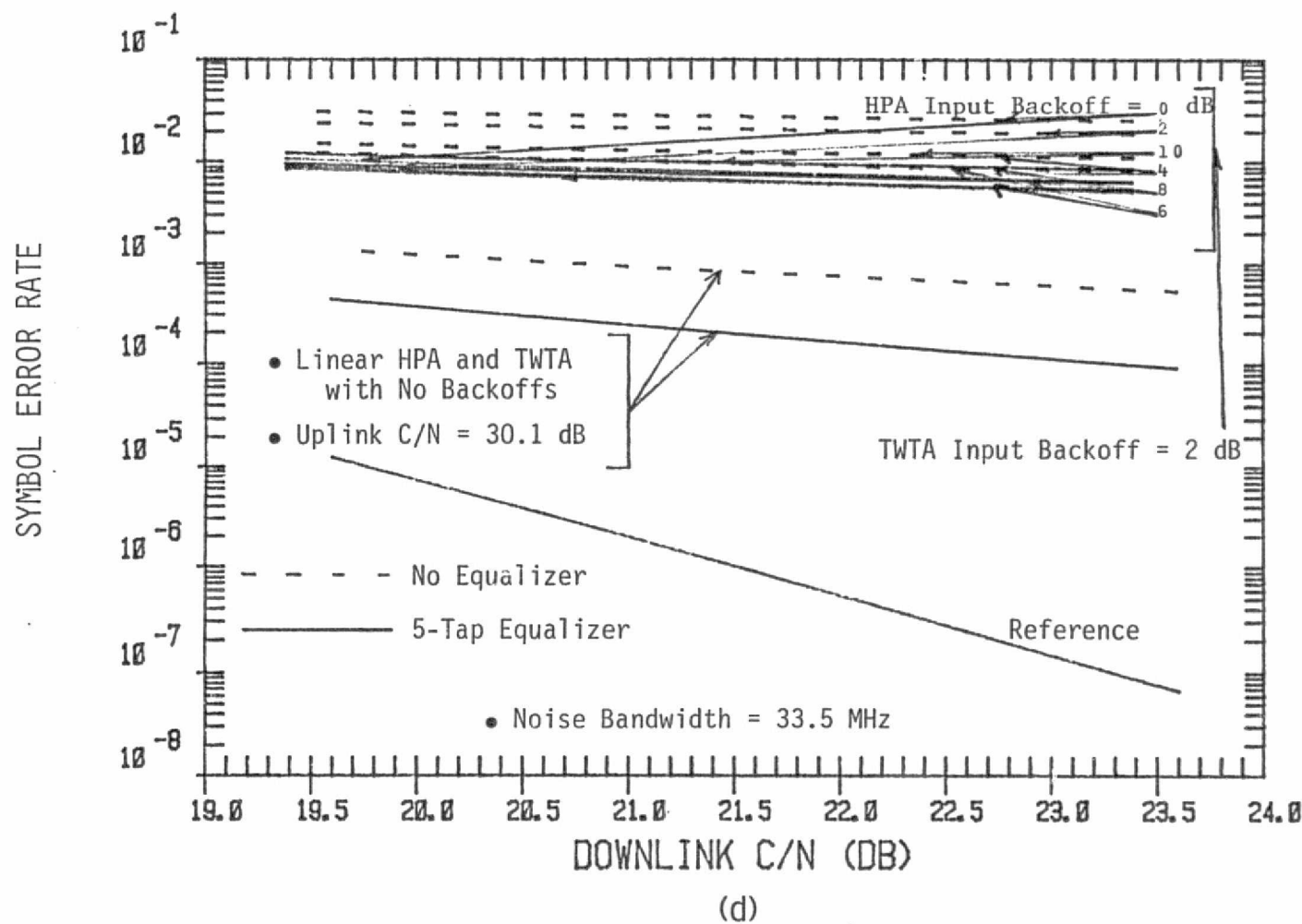
Figure 8. Simulated Performance of 8PSK at 97.1 Msps
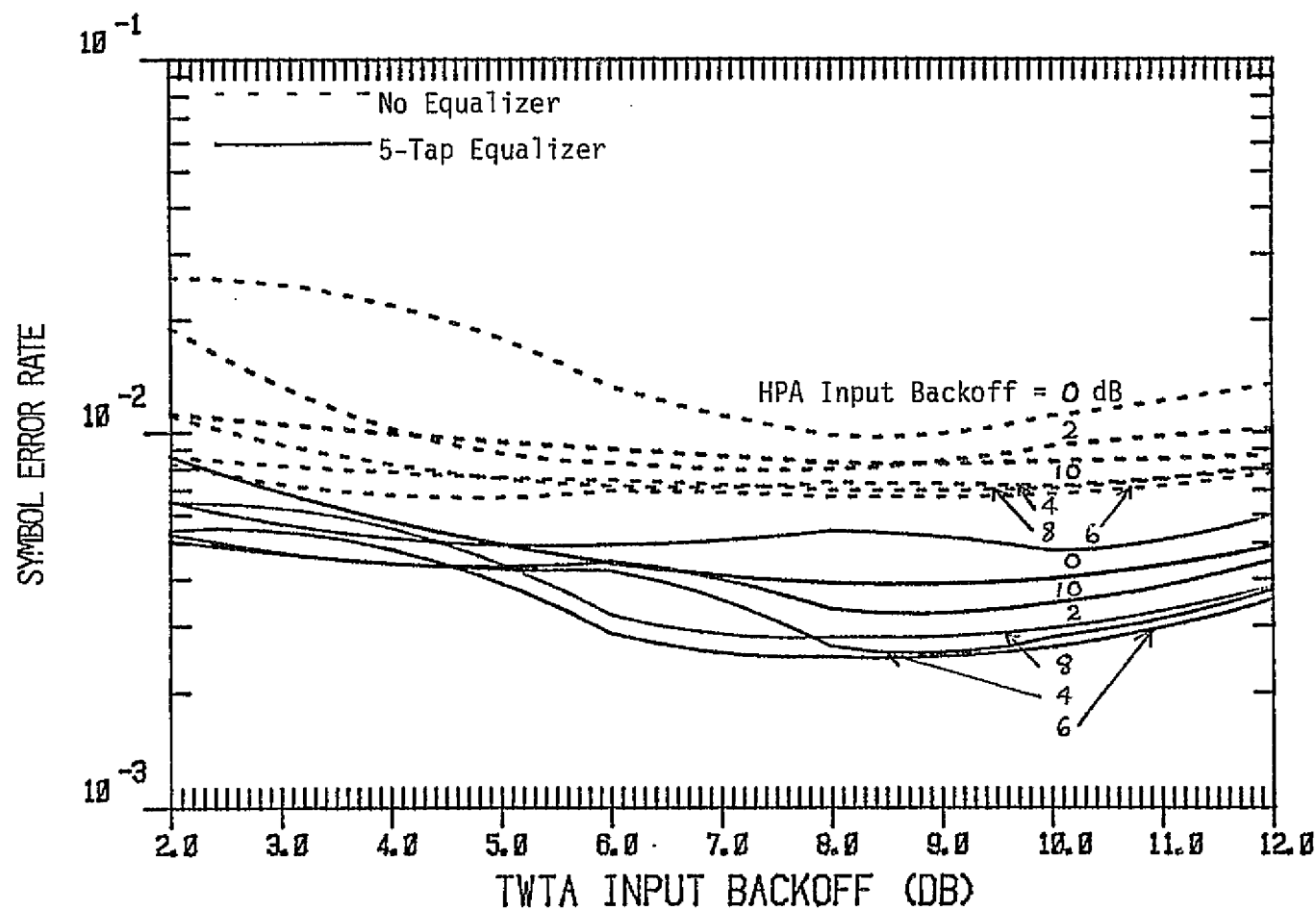
Figure 9.   Simulated Performance of 8PSK at 97.1 Msps as a Function of
            TWTA Backoff
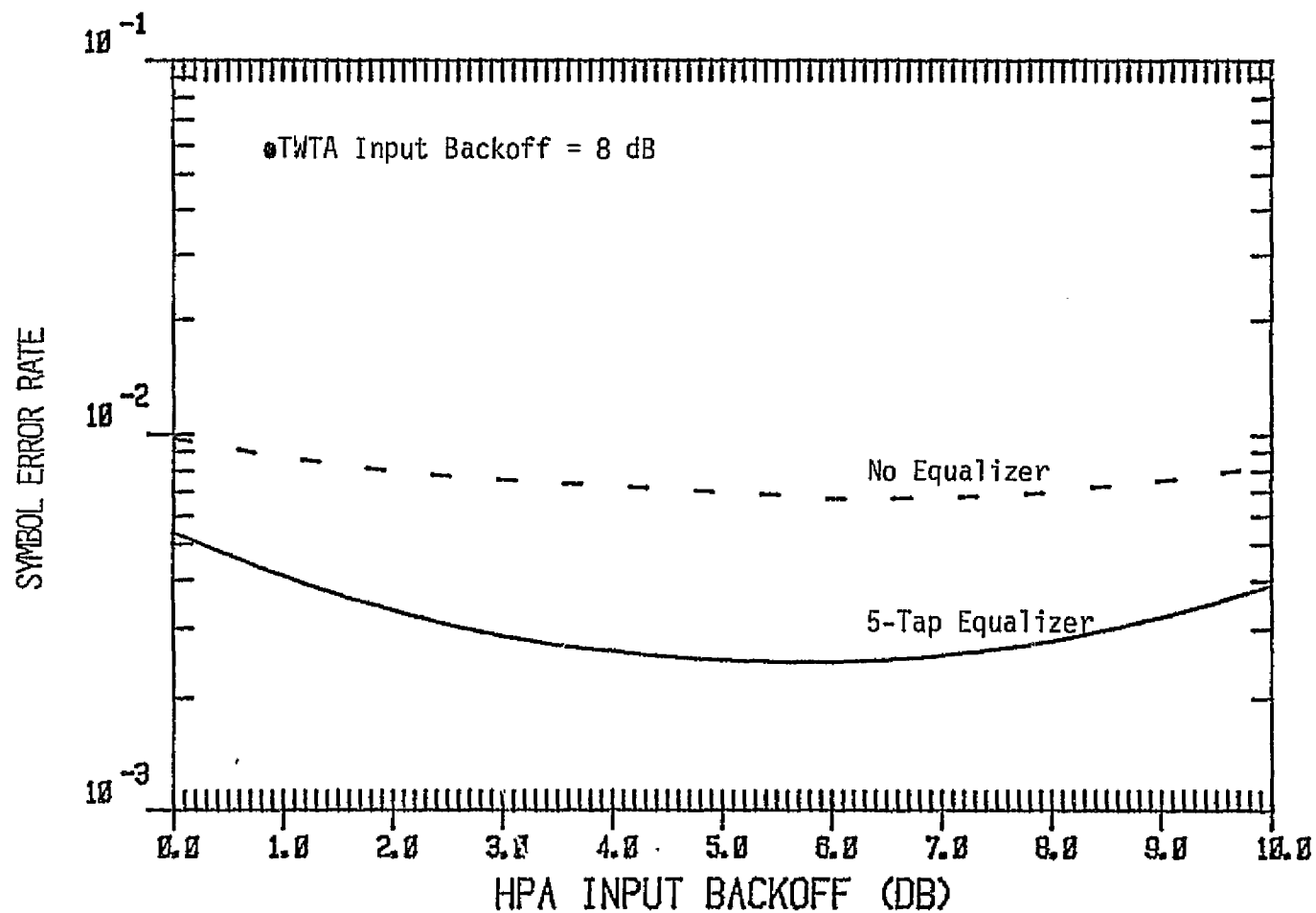
Figure 10. Simulated Performance of 8PSK at 97.1 Msps as a Function of HPA Backoff.

(a)

Figure 11.   Simulated Performance of 8PSK at 97.1 Msps with 3-Tap
Equalization

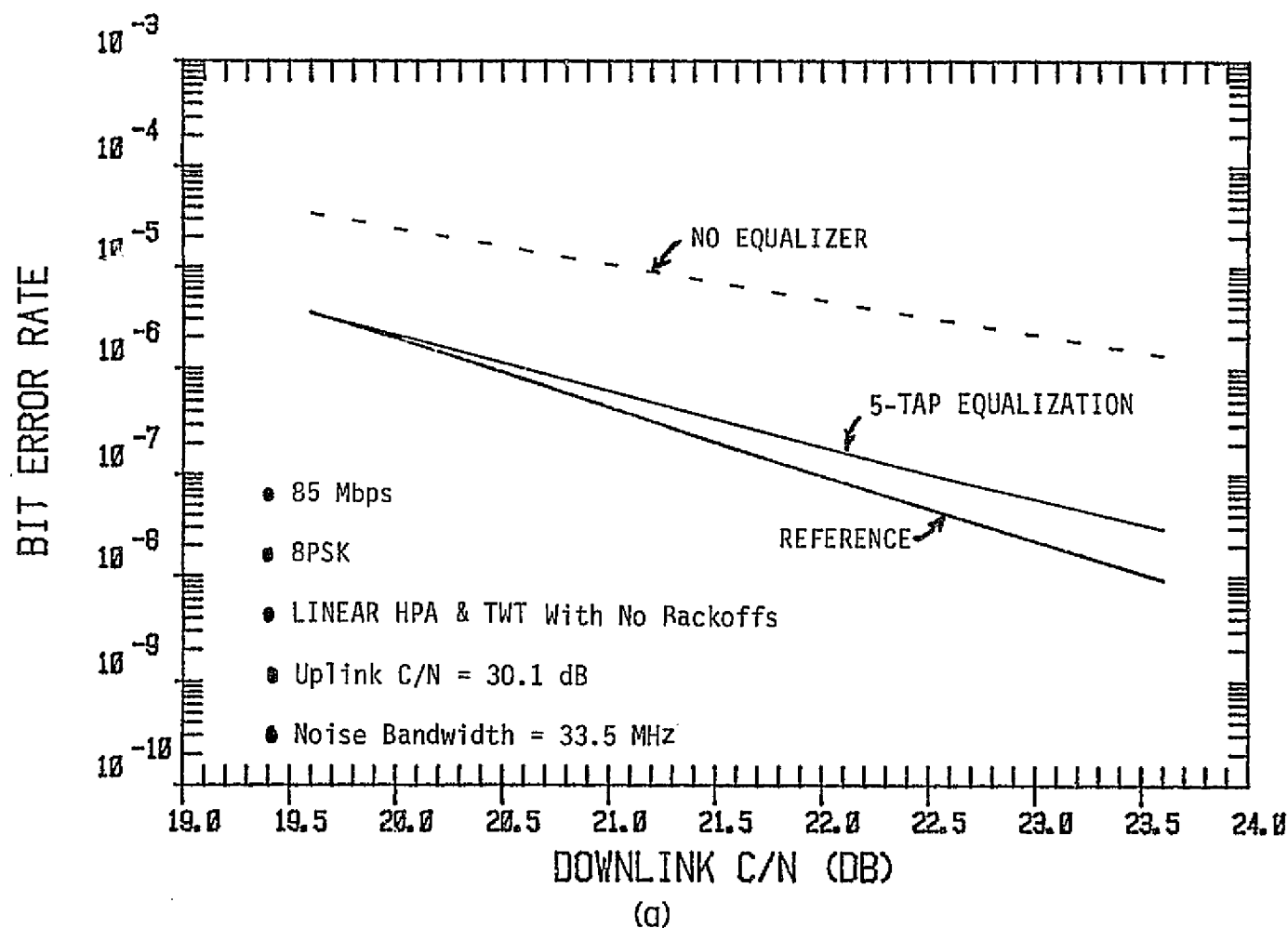Figure 11. Simulated Performance of 8PSK at 97.1 Msps with 3-Tap Equalization

Figure 11.   Simulated Performance of 8PSK at 97.1 Msps with 3-Tap
Equalization
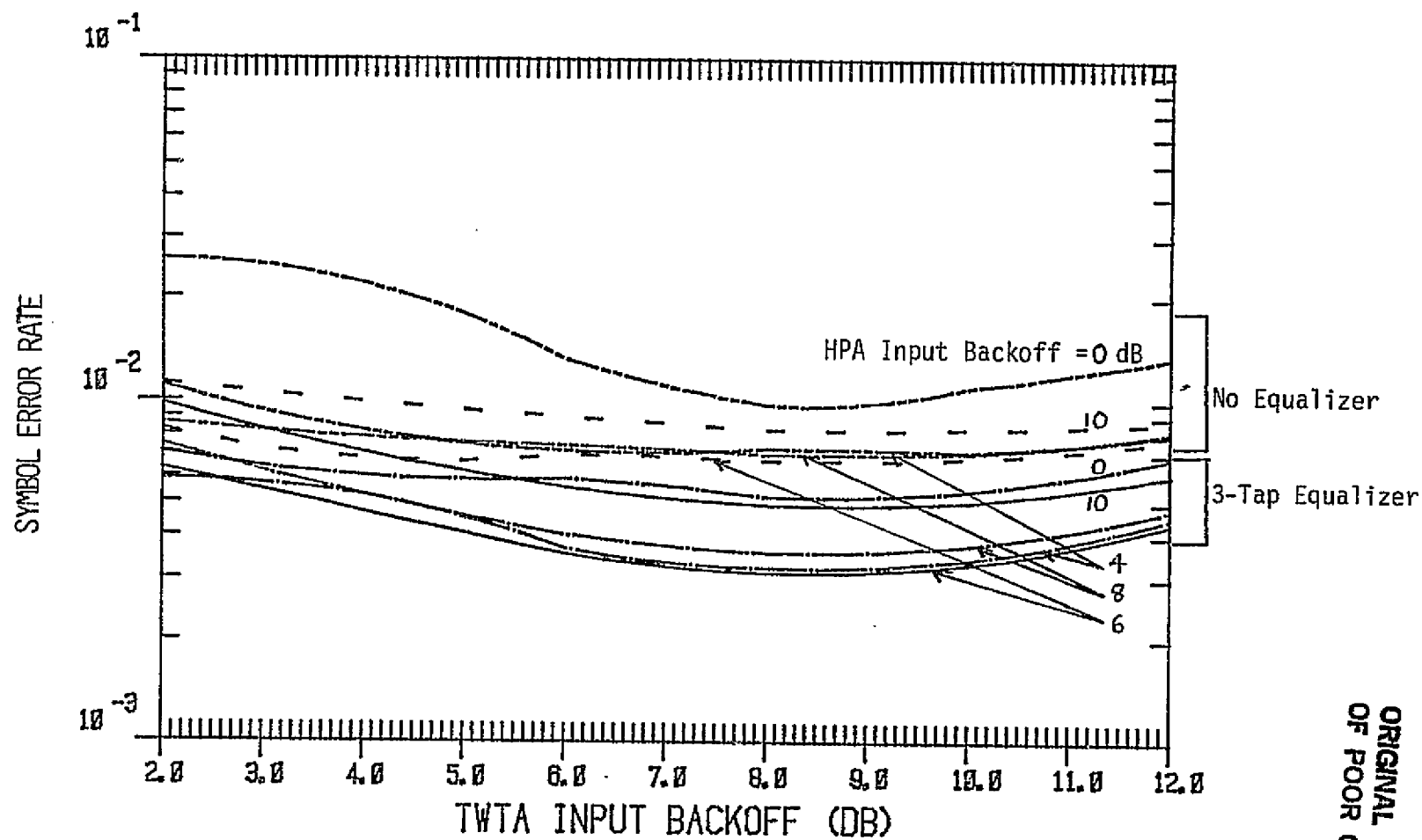
Figure 11. Simulated Performance of 8PSK at 97.1 Msps with 3-Tap
Equalization

Figure 11.   Simulated Performance of 8PSK at 97.1 Msps with 3-Tap
Equalization

Figure 12.   Simulated Performance of 8PSK at 85 Mbps Without Coding

Figure 12. Simulated Performance of 8PSK at 85 Mbps Without Coding

Figure 12.   Simulated Performance of 8PSK at 85 Mbps Without Coding

significantly affect the tradeoff between bandwidth conservation and noise and interference immunity. 8PSK is therefore used to illustrate the effect of each change on link performance.

The Chebyshev filters were the first channel elements to be altered (Figure 13). Although the phase distortion in the satellite channel filter is a potential source of ISI, this effect is alleviated by the larger channel bandwidth and, particularly, the large decrease in the ripple of each of the remaining four Chebyshev filters. The net effect is an 8PSK performance improvement, which can be observed by comparing Figures 14a through 14d with Fig. 8 and Figure 14e with Fig. 9.

Gain and phase response characteristics of the HPA and TWTA were also respecified. The HPA was assumed to be linear and the TWTA was replaced by the SSPA (Fig. 15). This change produces further performance improvement by reducing the signal distortion due to nonlinearity.

The final channel modification was the introduction of a sinusoidal term in the phase distortion model (Figure 16) to impose a ripple on the previous phase distortion characteristic in the satellite channel filter (Fig. 13). This causes a performance degradation at high system C/N_0 (carrier to noise density ratio) (Figures 17 and 18), because the SSPA phase distortion is large (Fig. 15).

3. Comparison of 8PSK and DBLP Performance and Out-of-Band Power

The revised channel model was used to compare the performance and out-of-band power of 8PSK with those of a simplified version of Motorola's DBLP modulation scheme. Although the channel model is the same for both modulations, the transmit and receive filter chains for the DBLP simulation are different from those of the 8PSK model (Figure

	Old Model[1]	New Model[2]
Transmit Channel Filter	W=38 MHz 4-pole	W=42 MHz 4-pole
HPA Output Filter	W=38 MHz 4-pole	W=42 MHz 4-pole
Satellite Input Channel Filter with Phase Distortion[3]	W=34 MHz 6-pole	W=39 MHz 3-pole
TWT Output Filter	W=34 MHz 3-pole	None
Receive Chain Filter	W=38 MHz 4-pole	W=3.6 MHz 4-pole

[1] Chebyshev with 1 dB peak-to-peak ripple , 3 dB Bandwidth W

[2] Chebyshev with 0.2 dB peak-to-peak ripple , 3 dB Bandwidth W

[3] Phase Distortion:

Phase Shift $\emptyset_1(f)$ in Radians

Offset f From
Center Frequency, MHz
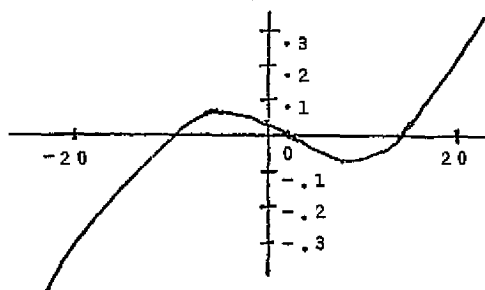
$$\emptyset_1(f)=\emptyset_0\left(-6\frac{[f-f_0]}{f_1} + 32\left[\frac{f-f_0}{f_1}\right]^3\right)$$

where f_0 = 2 MHz

f_1 = 28 MHz

$\emptyset_0$ = 0.06 radian
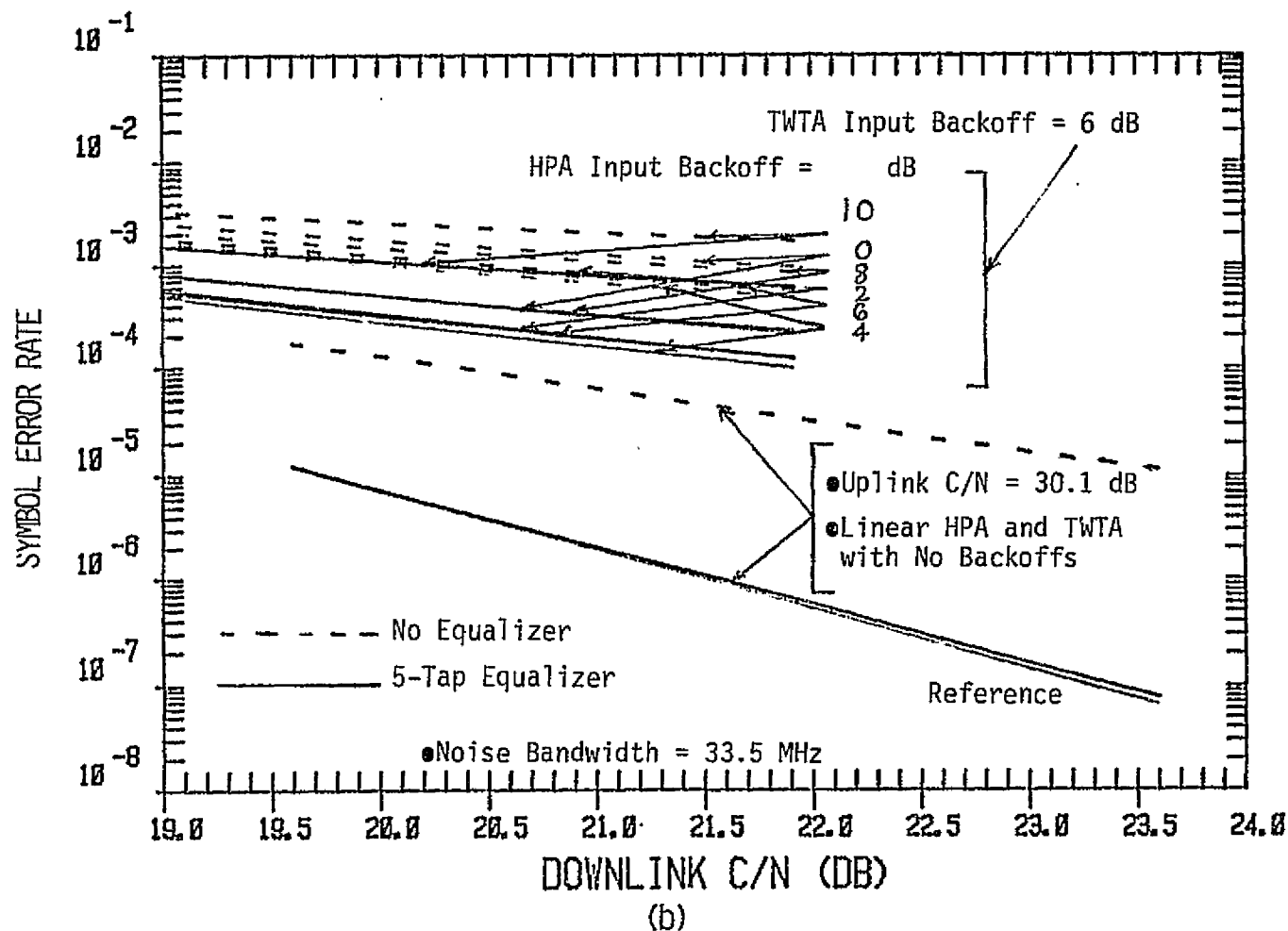
Figure 13. Revised Model of Channel Filters
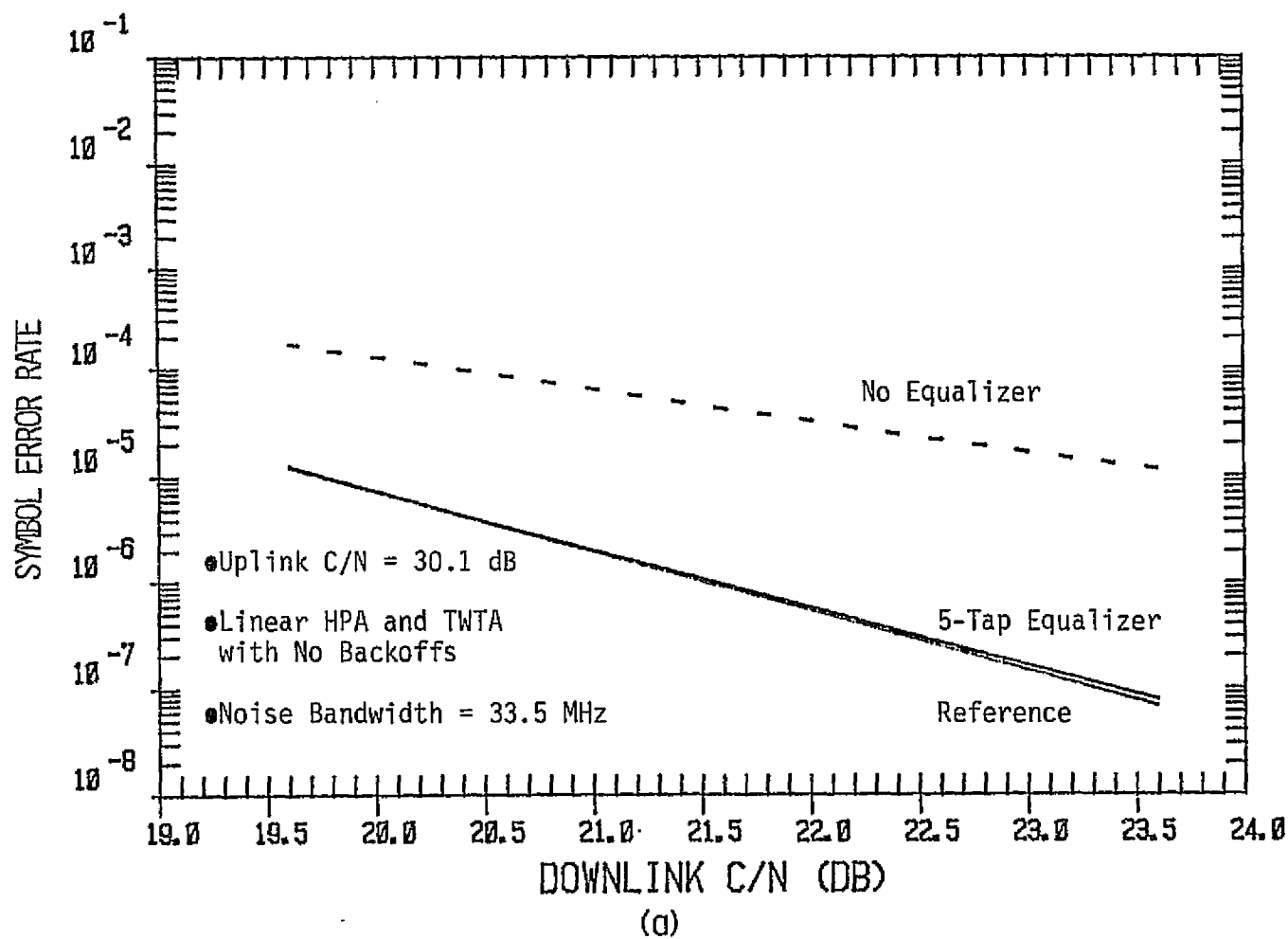
Figure 14. Simulated Performance of 8PSK at 97.1 Msps in Channel with Revised Filters

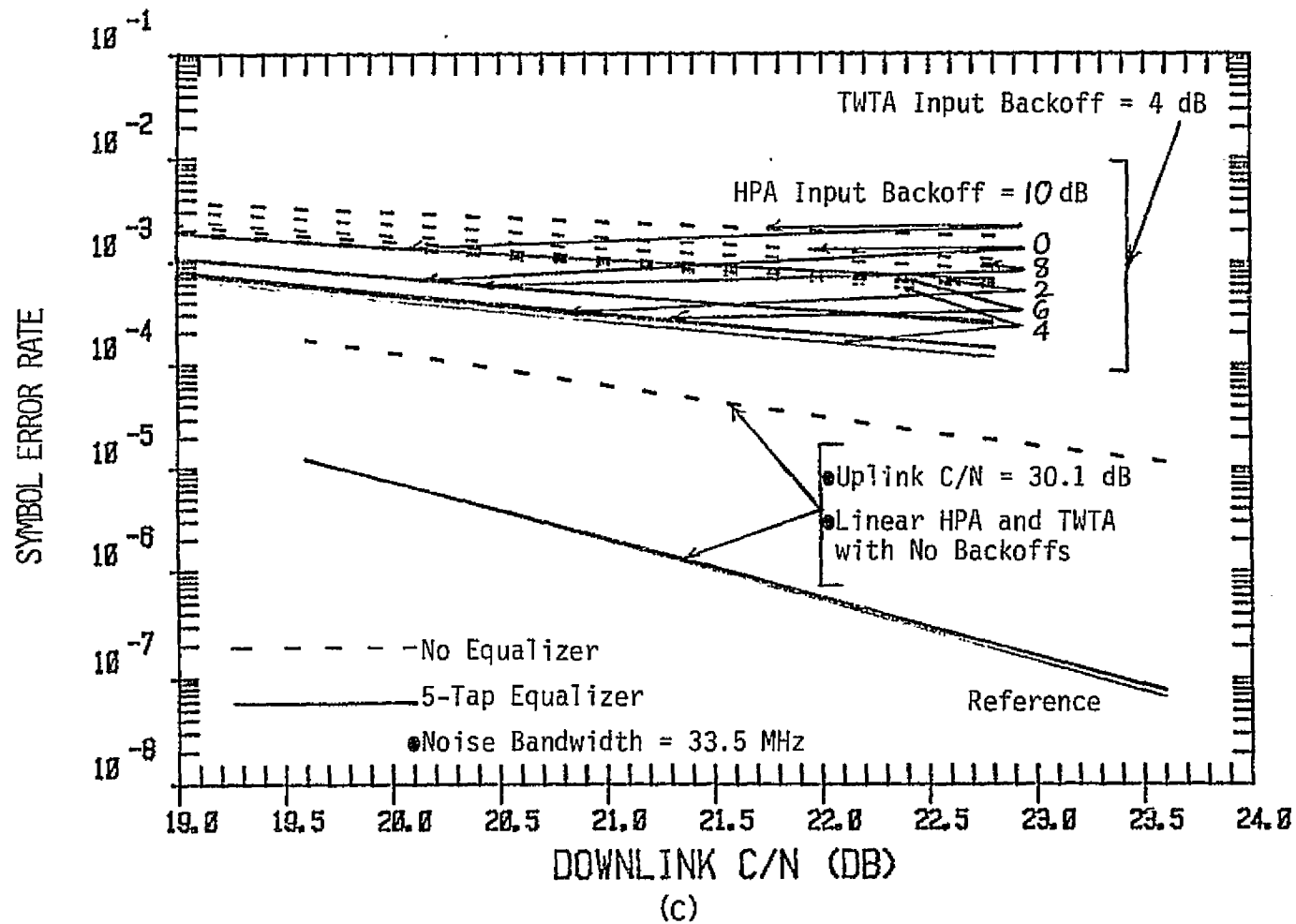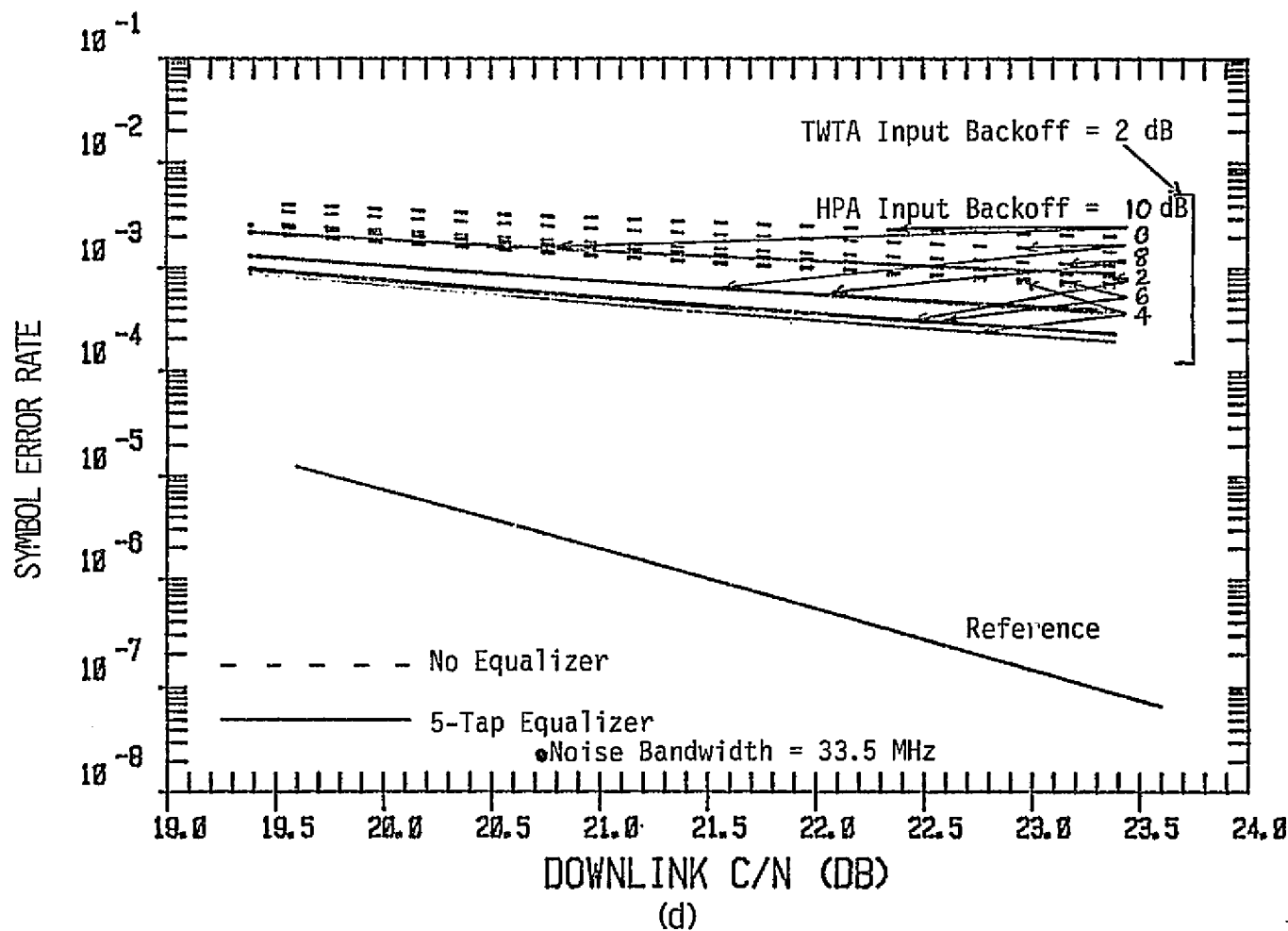Figure 14. Simulated Performance of 8PSK at 97.1 Msps in Channel with Revised Filters

Figure 14. Simulated Performance of 8PSK at 97.1 Msps in Channel with Revised Filters
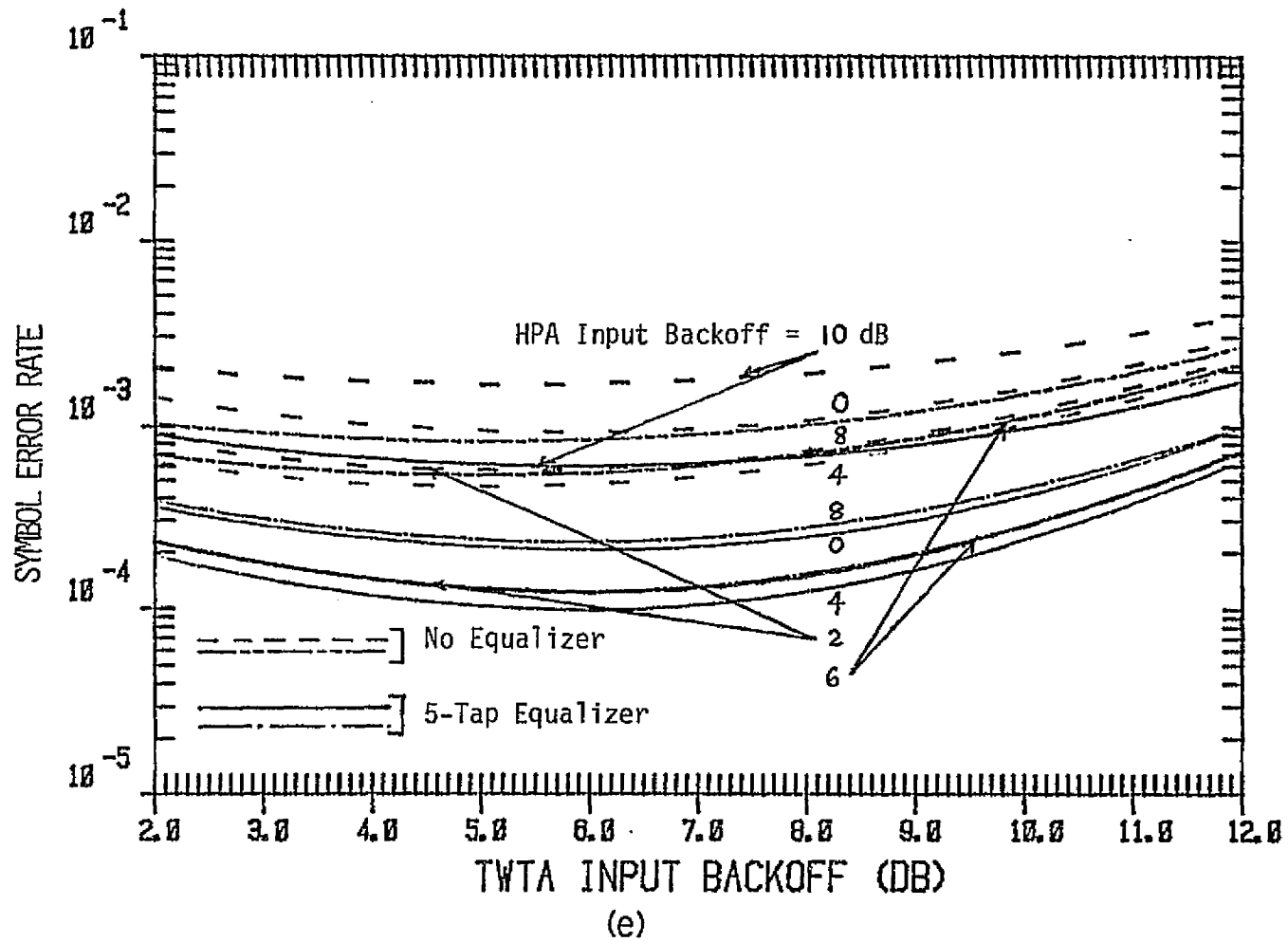
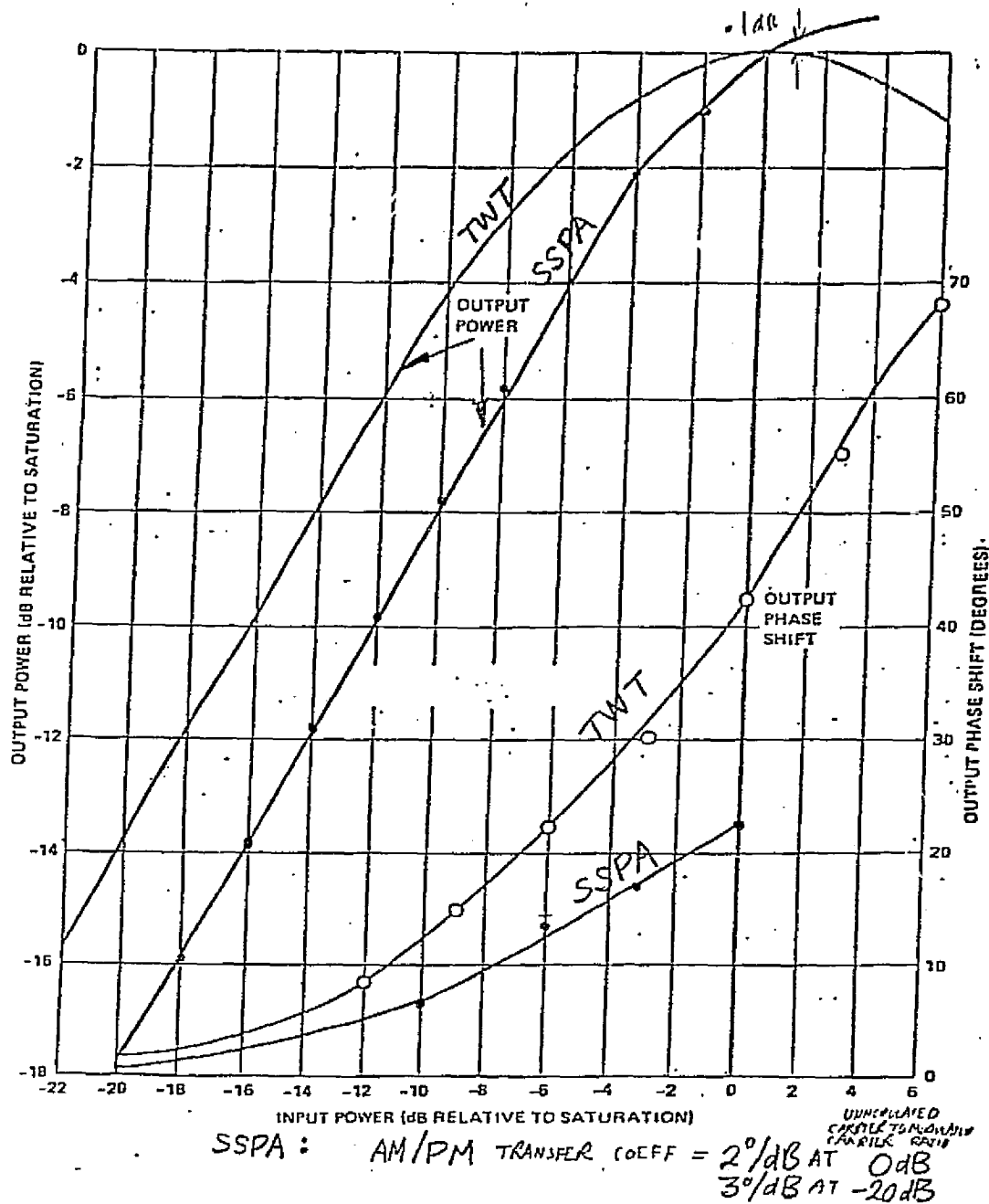Figure 14. Simulated Performance of 8PSK at 97.1 Msps in Channel with Revised Filters

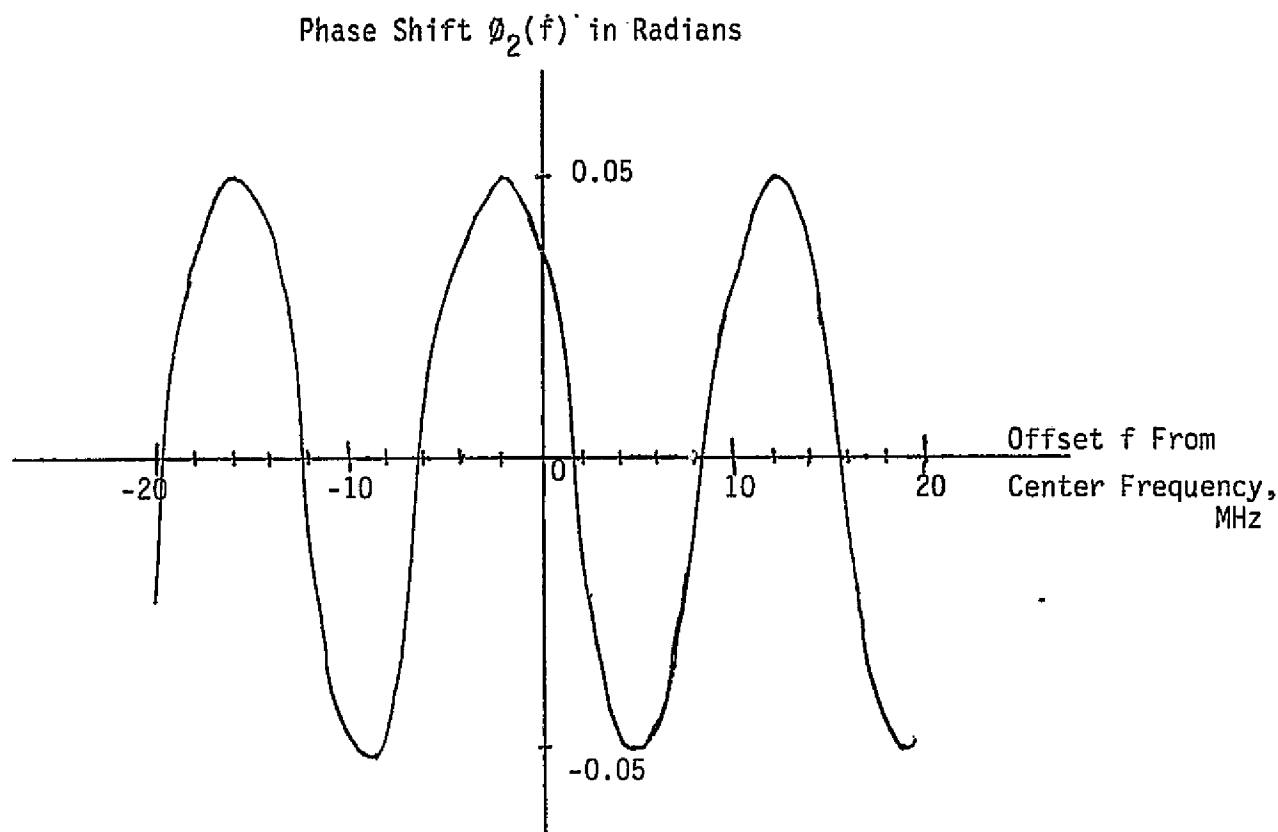Figure 14. Simulated Performance of 8PSK at 97.1 Msps in Channel with Revised Filters

Figure 15. Comparison of TWT and SSPA

Phase Shift $\emptyset_2(f)$ in Radians

$$\emptyset_2(f) = -\emptyset_3 \cos[2\pi(f-f_0)/f_1]$$

$$f_0 = 2 \text{ MHz}$$

$$f_1 = 28 \text{ MHz}$$

$$\emptyset_3 = 0.049 \text{ radian}$$

Figure 16.   Sinusoidal Phase Distortion Characteristic
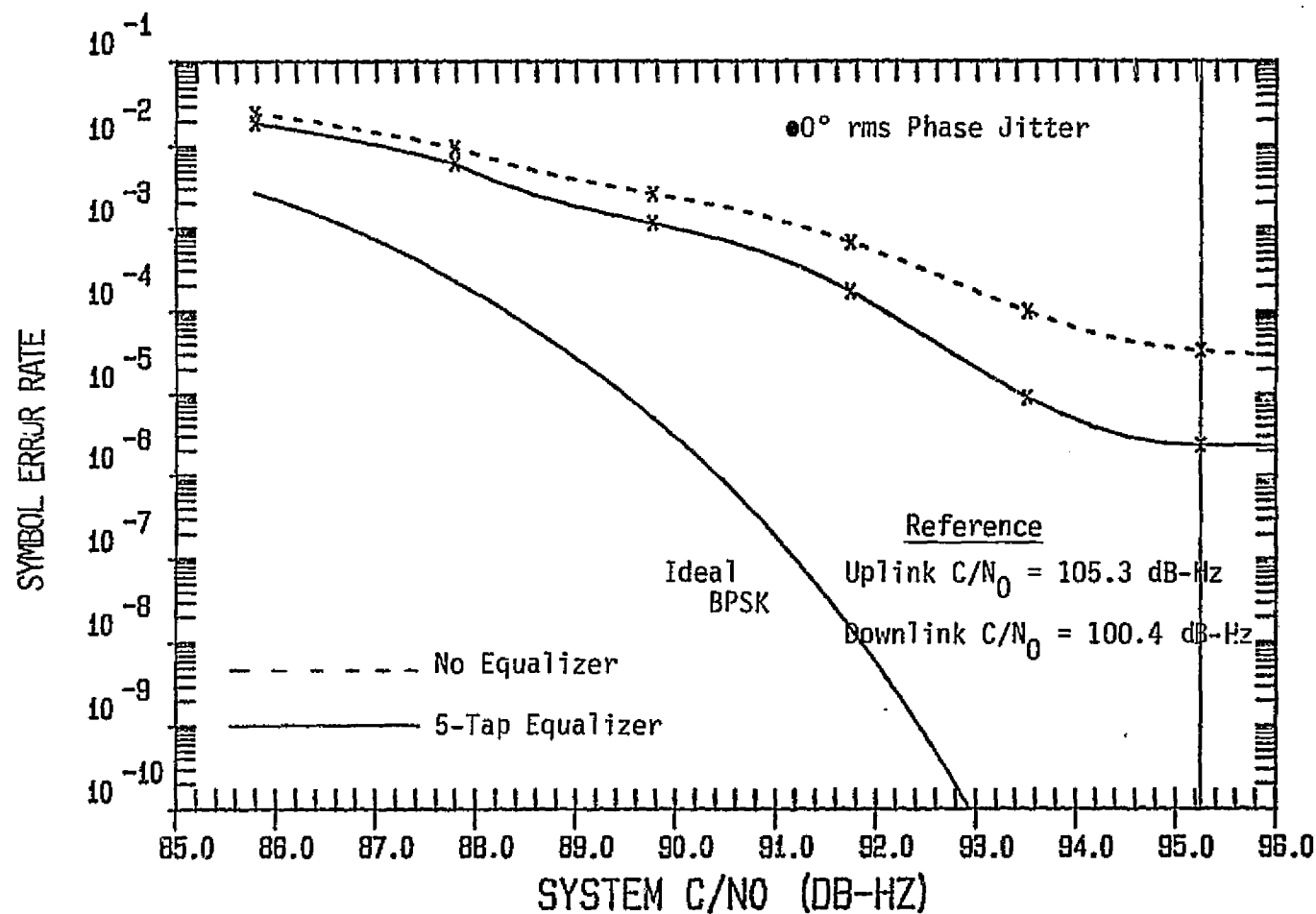to be Added to Phase Distortion in Satellite
Input Channel Filter

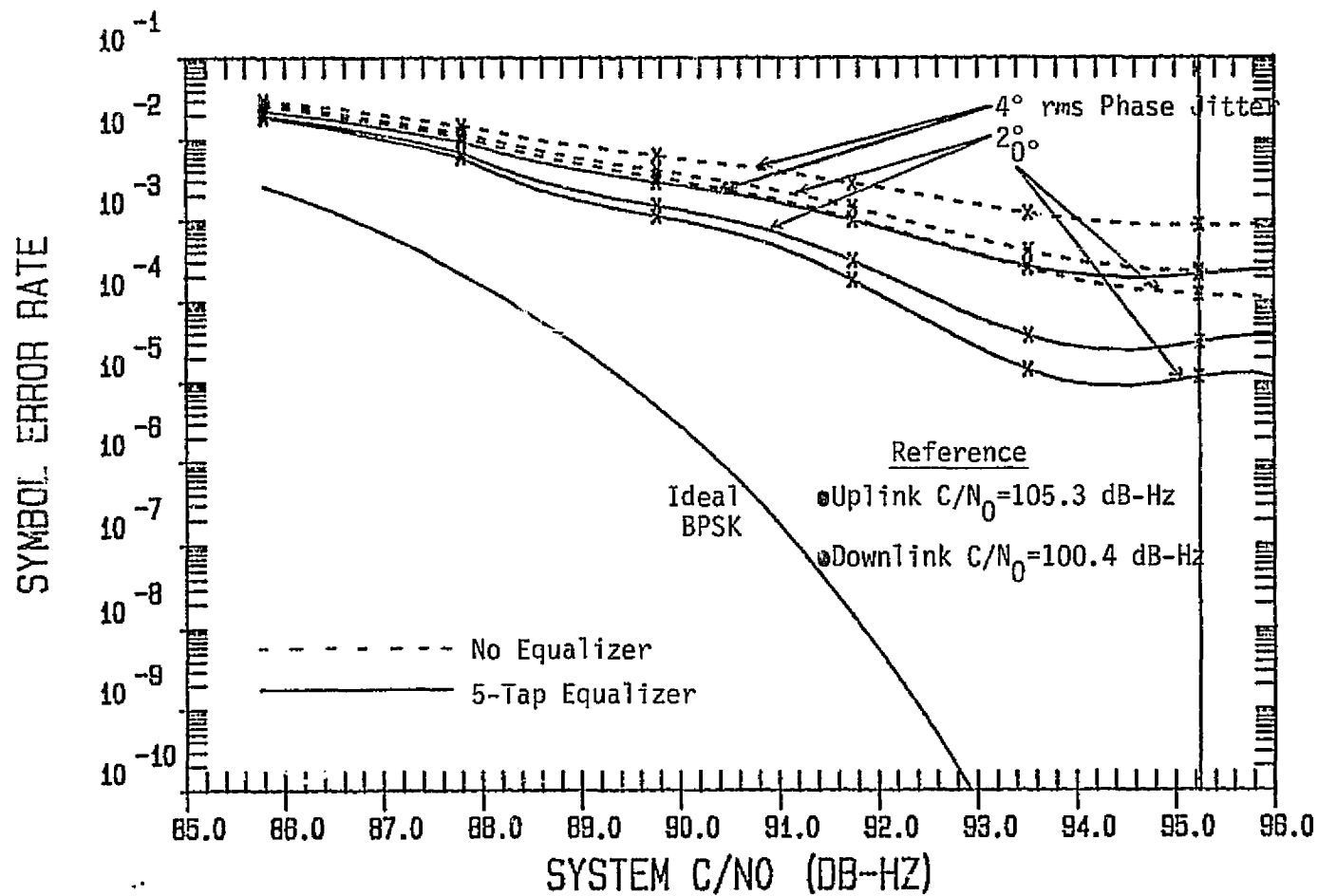Figure 17. Simulated Performance of 8PSK at 97.1 Msps without Sinusoidal Phase Distortion

Figure 18. Simulated Performance of 8PSK at 97.1 Msps in Channel with Sinusoidal Phase Distortion

1). In addition, the DBLP demodulator is based on the maximum likelihood detection algorithm with 3 symbol periods of memory.

The simulated DBLP modem outperforms 8PSK (even with equalization) on the SDT channel (Figures 18 and 19), but only at the cost of greater out-of-band power (Figure 20) at the output of the transmitter. 8PSK power drops off faster because each coded symbol may cause a DBLP phase transition, even though this transition is smooth.
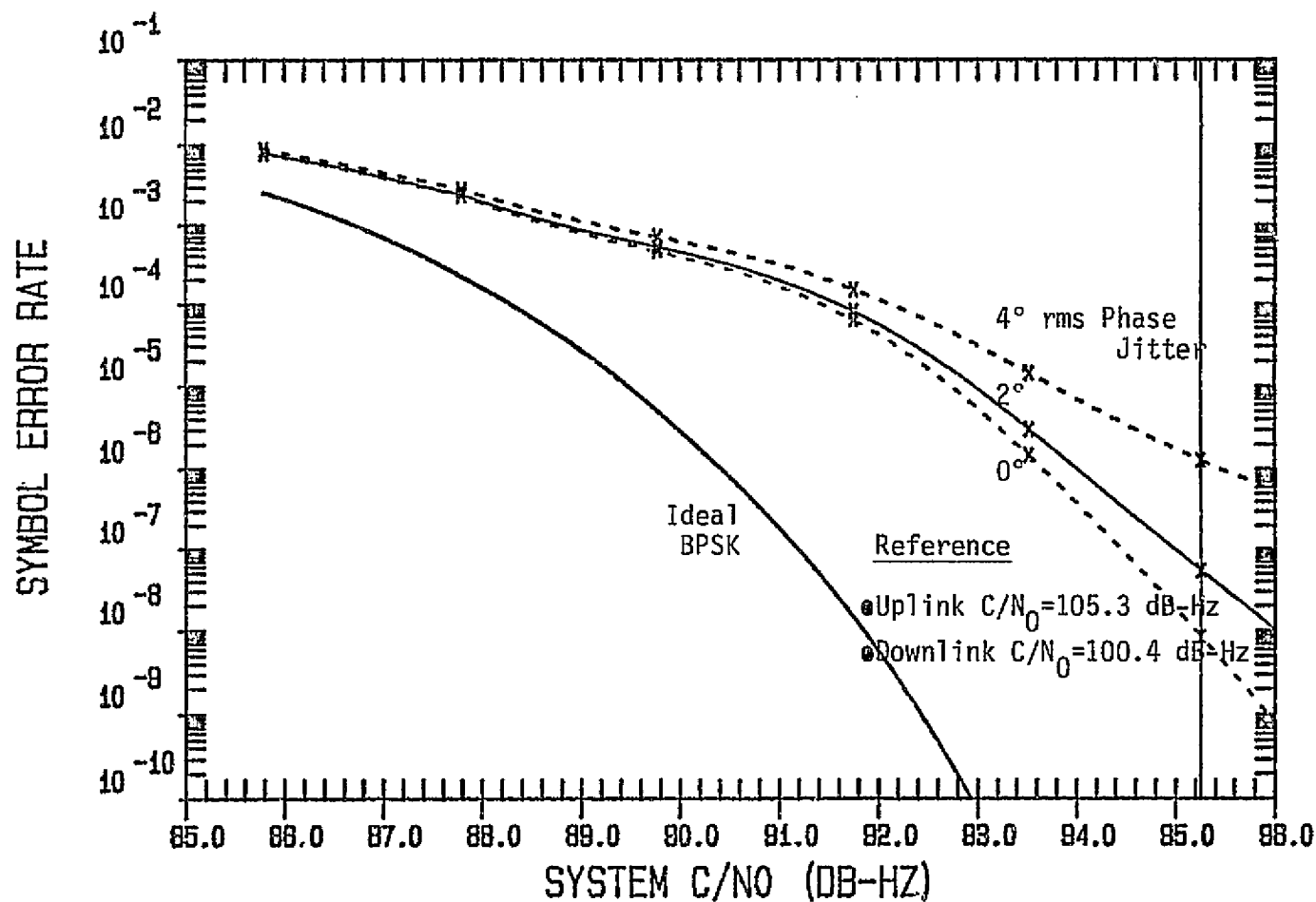
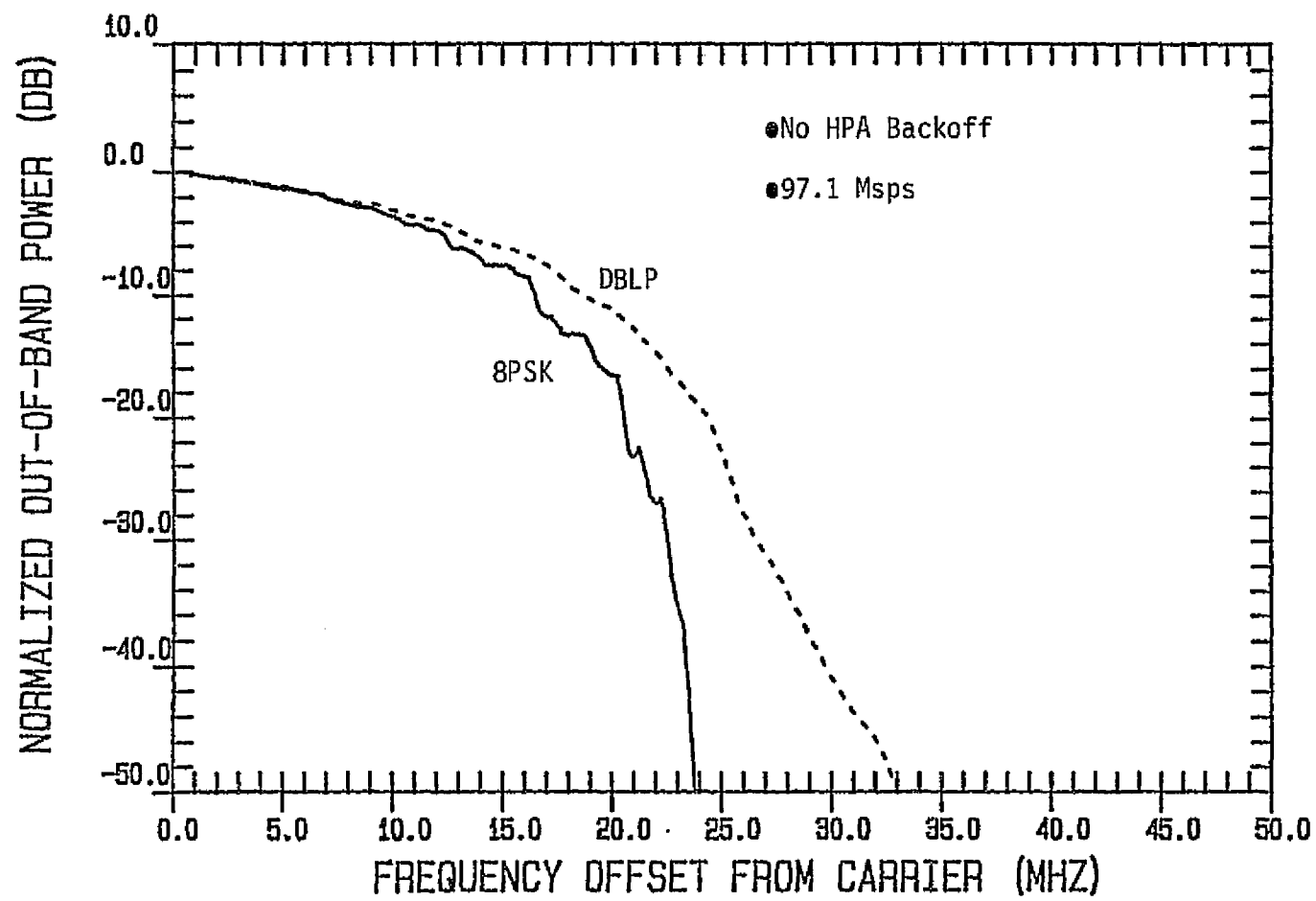Figure 19.   Simulated Performance of DBLP at 97.1 Msps

Figure 20.   Out-of-Band Power at the Output of the Transmitting Earth Terminal